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TITLE: DRIVING METHOD FOR PLASMA DISPLAY PANEL

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INVENTOR-INFORMATION:

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ABSTRACT:

PROBLEM TO BE SOLVED: To enhance contrast with low power consumption while suppressing a spurious profile also and moreover to enhance display quality by stabilizing selective discharge.

SOLUTION: In this method, either of a first mode in which the number of light emitting times of sustaining light emitting processes of respective SFs in SF(subfield) groups in the display period of one field is set to a first value or a second mode in which the number of light emitting times of sustaining light emitting processes of respective SFs in SF groups is set to a second value lower than the first value is selected and, at least one of the values of the pulse width and the pulse voltage of the scanning pulse is set so as to become larger as compared with values of the pulse width and the pulse voltage of the scanning pulse of respective SFs in SF groups at the time of selecting the first mode in respective SFs in SF groups when the second mode is selected.

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] This invention relates to the drive approach of the plasma display panel (PDP is called hereafter) of a matrix display method.
[0002]
[Description of the Prior Art] PDP of AC (alternating current discharge) mold is known as one of the PDP(s) of this matrix display method. PDP of AC mold is equipped with two or more line electrode pairs which intersect perpendicularly with two or more train electrodes (address electrode) and these trains electrode, and are arranged, and form 1 scan line in a pair. Each [these] line electrode pair and a train electrode are covered with the dielectric layer to discharge space, and have the structure where the discharge cel corresponding to 1 pixel is formed on the intersection of a line electrode pair and a train electrode.
[0003] Under the present circumstances, since PDP uses the discharge phenomenon, the above-mentioned discharge cel has only two conditions, "luminescence" and nonluminescent ["nonluminescent"]. Then, the subfield method is used in order to realize the brightness display of halftone in this PDP. By the subfield method, 1 field period is divided into the subfield of N individual, the luminescence period (count of luminescence) corresponding to weighting of each bit digit of pixel data (N bit) is assigned to each subfield, respectively, and a luminescence drive is performed to it.
[0004] For example, as shown in drawing 1 , when 1 field period is divided into six subfields SF1-SF6, a luminescence drive is carried out in the luminescence period ratio which becomes SF1:1SF2:2SF3:4SF4:8SF5:16SF6:32.
[0005] For example, when making light emit only in SF6 of the subfields SF1-SF6 when making a discharge cel emit light by brightness"32", and making light emit by brightness"31", light is made to emit in other subfields SF1-SF5 except a subfield SF 6. Thereby, the brightness expression of the halftone in 64 steps is attained. Here, the luminescence drive pattern within 1 field period has reversed the discharge cel like **** by the case where light is made to emit by the case where light is made to emit by 32", and brightness "brightness" 31." that is, the inside of 1 field period -- setting -- brightness -- during the period when the discharge cel which should be made to emit light by "32" is emitting light -- brightness -- the discharge cel which should be made to emit light by "31" -- a nonluminescent condition -- becoming -- this brightness -- during the period when the discharge cel which should be made to emit light by "31" is emitting light -- brightness -- the discharge cel which should be made to emit light by "32" will be in a nonluminescent condition.
[0006] Therefore, existence of the field where the discharge cel which should be made to emit light by this discharge cel which should be made to emit light by 32" and brightness "brightness" 31" adjoins mutually produces the case where vision of the false coutour is carried out into this field. That is, since only the nonluminescent condition of both [these] the discharge cel will be continuously seen when a look is turned to the direction of the discharge cel which should be made to emit light by brightness"31" just before the discharge cel which should be made to emit light by brightness"32" changes to a

luminescence condition from a nonluminescent condition, vision of the dark line comes to be carried out on both boundary. Therefore, this serves as false coutour which is unrelated to pixel data in any way, appears on a screen, and reduces display quality.
[0007] Moreover, as mentioned above, since PDP used the discharge phenomenon, it also had to carry out discharge (accompanied by luminescence) which is unrelated to the contents of a display, and had the problem of reducing the contrast of an image. Furthermore, in producing this PDP commercially now, it has been a general technical problem to realize a low power.
[0008]
[Problem(s) to be Solved by the Invention] This invention aims at offering the drive approach of a plasma display panel that it is made in order to solve the above-mentioned problem, improvement in contrast can be aimed at with a low power although false coutour is controlled, selection discharge can be stabilized further and improvement in display quality can be aimed at.
[0009]
[Means for Solving the Problem] The drive approach of the plasma display panel of this invention It has two or more train electrodes arranged by intersecting each of the line electrode pair arranged for every scan line, and a line electrode pair. It is the drive approach of making a gradation display to the plasma display panel which formed the discharge cel corresponding to 1 pixel on each intersection of the line electrode pair for every scan line, and two or more train electrodes. The display period of the 1 field is divided into the subfield of N (N is two or more integers) individual. M subfields (2 <=M<=N) in which it is located continuously of the subfields of N individual are made into a subfield group. The reset stroke which makes the discharge which initializes all discharge cels in the condition of a luminescence cel only in the subfield of the head section in a subfield group occur The pixel data write-in stroke which impresses a pixel data pulse to a train electrode, and impresses a scan pulse to one side of a line electrode pair in order synchronizing with the pixel data pulse in order to make the discharge which sets a discharge cel as a nonluminescent cel in any 1 subfield in a subfield group occur The maintenance luminescence stroke which makes the discharge only the count of luminescence corresponding to weighting of a subfield makes [discharge] only a luminescence cel emit [discharge] light in each subfield in a subfield group occur It performs, respectively. Either of the 2nd mode which set the count of luminescence in the maintenance luminescence stroke of each subfield in the 1st mode which set the count of luminescence in the maintenance luminescence stroke of each subfield in a subfield group as the 1st value, and a subfield group as the 2nd value lower than the 1st value is chosen. At the time of selection in the 2nd mode, at least one of the pulse width of a scan pulse and the values of a pulse voltage is compared with the pulse width of the scan pulse of each subfield in the subfield group at the time of selection in the 1st mode, and the value of a pulse voltage in each subfield in a subfield group. It is characterized by setting up so that it may become size.
[0010]
[Embodiment of the Invention] Hereafter, the example of this invention is explained to a detail, referring to a drawing. Drawing 2 is drawing showing the outline configuration of the plasma display equipment which carries out the luminescence drive of the plasma display panel (PDP is called hereafter) based on the drive approach by this invention.
[0011] In drawing 2 , according to the clock signal supplied from the drive control circuit 2, A/D converter 1 samples the input video signal of an analog, changes this into the 8-bit pixel data (input pixel data) D for every pixel, and supplies this to the data-conversion circuit 30. The drive control circuit 2 generates the clock signal over above-mentioned A/D converter 1, and the store and read-out signal over memory 4 synchronizing with the horizontal and Vertical Synchronizing signal in the above-mentioned input video signal. Furthermore, the drive control circuit 2 generates these various timing signals that should carry out drive control of address driver 6, 1st SASUTIN driver 7, and 2nd SASUTIN driver 8 each synchronizing with level and a Vertical Synchronizing signal.
[0012] The data-conversion circuit 30 changes these 8-bit pixel data D into the 14-bit conversion pixel data (display pixel data) HD, and supplies this to memory 4. In addition, about conversion actuation of this data-conversion circuit 30, it mentions later. Memory 4 writes in the above-mentioned conversion

pixel data HD one by one according to the write-in signal supplied from the drive control circuit 2. After the writing for one screen (n lines, m train) is completed by this write-in actuation, memory 4 divides and reads conversion pixel data HD11-nm for this one screen for every bit digit, and supplies this to the address driver 6 one by one for every one line.

[0013] the address driver 6 generates m pixel data pulses which have an electrical potential difference corresponding to the logical level of each conversion pixel data bit for one line read from this memory 4 according to the timing signal supplied from the drive control circuit 2, and impresses these to the train electrodes D1-Dm of PDP10, respectively. PDP10 is equipped with the above-mentioned train electrodes D1-Dm as an address electrode, and the line electrodes X1-Xn and the line electrodes Y1-Yn which are arranged by intersecting perpendicularly with these trains electrode. In PDP10, the line electrode which corresponded to one line in the pair of these line electrode X and the line electrode Y is formed. That is, the line electrode pairs of the 1st line in PDP10 are the line electrodes X1 and Y1, and the line electrode pairs of the n-th line are the line electrodes Xn and Yn. The top Noriyuki electrode pair and the train electrode are covered with the dielectric layer to discharge space, and have the structure where the discharge cel corresponding to 1 pixel is formed on the intersection of each line electrode pair and a train electrode.

[0014] According to the timing signal supplied from the drive control circuit 2, although 1st SASUTIN driver 7 and 2nd SASUTIN driver 8 each is explained below, it generates **** various driving pulses, and it impresses these to the line electrodes X1-Xn of PDP10, and Y1-Yn. In this plasma display equipment, according to the timing signal supplied from the drive control circuit 2, as shown in drawing 3 , the drive to PDP10 divides the display period of the 1 field into 14 subfields SF1-SF14, and is performed.

[0015] Drawing 4 is drawing showing the internal configuration of this data-conversion circuit 30. In drawing 4 , the ABL (automatic brightness control) circuit 31 adjusts an intensity level to the pixel data D for every pixel by which sequential supply is carried out from A/D converter 1, and supplies the brilliance-control pixel data DBL obtained at this time to the 1st data-conversion circuit 32 so that the average luminance of the image displayed on the screen of PDP10 may fall within a predetermined brightness range.

[0016] Adjustment of this intensity level is performed, before setting up the ratio of the count of luminescence of a subfield nonlinear and performing a reverse gamma correction like ****. Therefore, the ABL circuit 31 performs a reverse gamma correction to the pixel data (input pixel data) D, and it is constituted so that it may carry out regulating automatically of the intensity level of the above-mentioned pixel data D according to the average luminance of the reverse gamma conversion pixel data obtained at this time. This prevents degradation of the display quality by the brilliance control.

[0017] Drawing 5 is drawing showing the internal configuration of this ABL circuit 31. In drawing 5 , the level equalization circuit 310 outputs the brilliance-control pixel data DBL which adjusted the level of the pixel data D and were obtained according to the average luminance for which the average luminance detector 311 mentioned later asked. The data-conversion circuit 312 is supplied to the average intensity-level detector 311 by using as the reverse gamma conversion pixel data Dr what changed these brilliance-control pixel data DBL in the reverse gamma property (Y=X2.2) which consists of a **** nonlinear characteristic although shown in drawing 6 . That is, the pixel data (reverse gamma conversion pixel data Dr) corresponding to the original video signal of which the gamma correction was canceled are restored by performing a reverse gamma correction to the brilliance-control pixel data DBL in the data-conversion circuit 312.

[0018] Although the average luminance detector 311 is shown in drawing 7 in order to specify the luminescence period (count of luminescence) in each subfield for example, it chooses the brightness mode which can carry out the luminescence drive of PDP10 from the 1st mode of ****, and the 2nd mode by the brightness according to the average luminance for which it asked like ****, and it supplies brightness mode signal LC which shows this selected brightness mode to the drive control circuit 2. Under the present circumstances, although the drive control circuit 2 is shown in drawing 7 R> 7, it sets up the number of the maintenance pulses impressed in the subfield SF 1 shown in drawing 3 - SF14 the

period Ic which carries out luminescence maintenance in each maintenance luminescence stroke Ic, i.e., each maintenance luminescence stroke, according to the count ratio of luminescence for every mode specified in **** brightness mode signal LC. That is, the average intensity level of the input pixel data D is set as the 1st mode of the above under with a predetermined value, when an average intensity level becomes beyond a predetermined value, it switches to the 2nd mode fewer than the case where the count of luminescence of each subfield is the 1st mode, and brightness is restricted automatically.

[0019] Moreover, the average luminance detector 311 is supplied to the above-mentioned level equalization circuit 310 in quest of the average luminance from the above-mentioned reverse gamma conversion pixel data Dr. Although the 1st data-conversion circuit 32 in drawing 4 is shown in drawing 8 , it is changed into the 8 bits (0-224) conversion pixel data HDp which set the brilliance-control pixel data DBL of 256 gradation (8 bits) to 14x16 / 255 (224/255) based on the **** transfer characteristic, and is supplied to the many gradation-ized processing circuit 33. Although specifically shown in drawing 9 and drawing 10 based on the transfer characteristic which requires the 8 bits (0-255) brilliance-control pixel data DBL, it is changed according to a **** translation table. That is, this transfer characteristic is the number of bits of input pixel data. It is set up according to the compression number of bits and the number of display gradation by the formation of many gradation. Thus, the 1st data-conversion circuit 32 is established in the preceding paragraph of the many gradation-ized processing circuit 33 mentioned later, conversion doubled with the number of display gradation and the compression number of bits by the formation of many gradation performs, this carves a high-order-bit group (it corresponds to many gradation-ized pixel data), and a lower bit group (data omitted: error data) for brilliance-control pixel data DBL on a bit boundary, and many gradation-ized processing performs based on this signal. Generating (namely, generating of gradation distortion) of the flat part of the display property produced by this when there are no generating and display gradation of brightness saturation by many gradation-ized processing in a bit boundary can be prevented.

[0020] In addition, although the number of gradation will decrease since a lower bit group is omitted, the decrement of the number of gradation is made to be obtained by actuation of the many gradation-ized processing circuit 33 explained below in false. Drawing 11 and drawing 12 are drawings showing the impression timing of the various driving pulses which above-mentioned address driver 6, 1st SASUTIN driver 7, and 2nd SASUTIN driver 8 each impresses to the train electrodes D1-Dm of PDP10, the line electrodes X1-Xn, and Y1-Yn according to this luminescence drive format.

[0021] In the example shown in drawing 11 , as shown in drawing 3 , the display period of the 1 field is divided into 14 subfields SF1-SF14, and the drive to PDP10 is performed in the brightness mode in the 1st mode. In the example shown in drawing 12 , the same drive is performed in the brightness mode in the 2nd mode. In each subfield, the pixel data write-in stroke Wc which writes in pixel data to each discharge cel of PDP10, and performs a setup of a luminescence cel and a nonluminescent cel, and the maintenance luminescence stroke Ic which carries out luminescence maintenance only of the above-mentioned luminescence cel are carried out. Moreover, the simultaneous reset stroke Rc which makes all the discharge cels of PDP10 initialize in the top subfield SF 1 is performed, and the elimination stroke E is performed in the subfield SF 14 at the tail end.

[0022] Here, in the above-mentioned simultaneous reset stroke Rc, although the 1st SASUTIN driver 7 and the 2nd SASUTIN driver 8 are shown in drawing 11 and drawing 12 to the line electrodes X1-Xn of PDP10 and Y1 - Yn(s) of each, they impress the **** reset pulses RPx and RPY to coincidence. Thereby, reset discharge of all the discharge cels in PDP10 is carried out, and predetermined wall charge is uniformly formed in each discharge cel. Thereby, all the discharge cels in PDP10 turn into a luminescence cel in which a luminescence condition is maintained in the maintenance luminescence stroke mentioned later.

[0023] It is impressed by the train electrodes D1-Dm one by one, and the address driver 6 goes pixel data pulse group DP11-n for every line, DP21-n, DP31-n, ..., DP141-n by each pixel data write-in stroke Wc, as shown in drawing 1111 and drawing 12 . that is, the address driver 6 -- the inside of a subfield SF 1 -- above-mentioned conversion pixel data HD11-nm -- as it is shown in drawing 11 R> 1 and drawing 12 , for every one line, it is impressed by the train electrodes D1-Dm one by one, and goes

pixel data pulse group DP11-n corresponding to - of 1st line the n-th line of each generated based on each 1st bit. moreover -- the inside of a subfield SF 2 -- above-mentioned conversion pixel data HD11-nm -- as it is shown in drawing 11 and drawing 12 , for every one line, it is impressed by the train electrodes D1-Dm one by one, and goes pixel data pulse group DP21-n generated based on each 2nd bit. Under the present circumstances, the address driver 6 is restricted when the bit logic of conversion pixel data is logical level "1", it generates the pixel data pulse of the high voltage, and impresses it to the train electrode D. Although shown in drawing 11 and drawing 12 , the 2nd SASUTIN driver 8 generates the **** scan pulse SP, carries out sequential impression of this to the line electrodes Y1-Yn, and goes by the same timing as the impression timing of each pixel data pulse group DP. Under the present circumstances, discharge (selection elimination discharge) arises only in the discharge cel of the intersection of the "line" to which the scan pulse SP was impressed, and the "train" to which the pixel data pulse of the high voltage was impressed, and the wall charge which remained in that discharge cel is eliminated alternatively. By this selection elimination discharge, the discharge cel initialized by the condition of a luminescence cel in the above-mentioned simultaneous reset stroke Rc changes to a nonluminescent cel. In addition, discharge does not occur in the discharge cel currently formed in the "train" to which the pixel data pulse of the above-mentioned high voltage was not impressed, but the condition initialized in the above-mentioned simultaneous reset stroke Rc, i.e., the condition of a luminescence cel, is maintained.

[0024] That is, the luminescence cel in which a luminescence condition is maintained in the maintenance luminescence stroke mentioned later by activation of the pixel data write-in stroke Wc, and a nonluminescent [that it continues being in a putting-out-lights condition] cel are alternatively set up according to pixel data, and it succeeds in the writing of pixel data to each so-called discharge cel. Although the scan pulse SP is generated in order of the line electrodes Y1-Yn every subfields SF [SF1-] 14, it is the largest, a more nearly next subfield becomes small in time, and the pulse width of the scan pulse SP is the smallest in the subfield SF 14 in the subfield SF 1. That is, as shown at drawing 11 in the case of the 1st mode, when pulse width of the scan pulse SP corresponding to subfield SF 1 - SF14 each is set to Ta1-Ta14, it is Ta1>Ta2>Ta3>Ta4>..... There is relation like >Ta12>Ta13>Ta14. Moreover, as shown in drawing 12 similarly [in the case of the 2nd mode], when pulse width of the scan pulse SP corresponding to subfield SF 1 - SF14 each is set to Tb1-Tb14, it is Tb1>Tb2>Tb3>Tb4>..... There is relation like >Tb12>Tb13>Tb14. Furthermore, the thing in the 2nd mode of the pulse width of the scan pulse SP of each same subfield is size from the 1st mode. That is, there are Tb1>Ta1, Tb2>Ta2, Tb3>Ta3, ..., relation like Tb13>Ta13 and Tb14>Ta14.

[0025] In each maintenance luminescence stroke Ic, the 1st SASUTIN driver 7 and the 2nd SASUTIN driver 8 impress the maintenance pulses IPX and IPY by turns, as shown in drawing 11 and drawing 12 to the line electrodes X1-Xn, and Y1-Yn. Under the present circumstances, according to the above-mentioned pixel data write-in stroke Wc, during the period when these maintenance pulses IPX and IPY are impressed by turns, the discharge cel which is that wall charge remained with as, i.e., a luminescence cel, repeats electroluminescence, and it maintains that luminescence condition. Let pulse width Tsx1 of the maintenance pulse IPX 1 first impressed to the line electrodes X1-Xn in subfield SF 1 - SF14 each be size compared with the pulse width Tsx2 of the maintenance pulse IPX 2 after it - IPXi - Tsxi.

[0026] In addition, the maintenance periods of luminescence carried out in this maintenance luminescence stroke Ic differ for every subfield, as shown in drawing 3 . The count of luminescence in the maintenance luminescence stroke Ic in the 1st mode and the 2nd mode is as having been shown in drawing 7 . That is, it is non-linearity (namely, a reverse gamma ratio, Y=X2.2) about the ratio of the count of luminescence of each subfields SF1-SF14. It sets up so that it may change, and he is trying for this to amend the nonlinear characteristic (gamma property) of the input pixel data D.

[0027] Moreover, as shown in drawing 11 and drawing 12 , in the elimination stroke E in the subfield at the tail end, the address driver 6 generates blanking pulse AP, and impresses this to each of train electrode D1-m. The 2nd SASUTIN driver 8 generates blanking pulse EP in the impression timing and coincidence of this blanking pulse AP, and impresses this to the line electrode Y1 - Yn(s) of each. By coincidence impression of these blanking pulses AP and EP, elimination discharge occurs in [all / in

PDP10] a discharge cel, and the wall charge which remains in all discharge cels disappears. That is, all the discharge cels in PDP10 turn into a nonluminescent cel by this elimination discharge.
[0028] Although drawing 13 is shown in drawing 11 and drawing 12 , it is drawing showing all the patterns of the luminescence drive carried out based on a **** luminescence drive format. As shown in drawing 13 , it has set in the pixel data write-in stroke Wc in one subfield among subfields SF1-SF14, and selection elimination discharge is carried out to each discharge cel with a chisel (a black dot shows). That is, the wall charge formed in all the discharge cel of PDP10 of activation of the simultaneous reset stroke Rc remains until the above-mentioned selection elimination discharge is carried out, and in the maintenance luminescence stroke Ic in subfield SF in each which exists between them, electroluminescence is urged to it (with a circle [white] shows). That is, each discharge cel turns into a luminescence cel, and although shown in drawing 3 , it continues luminescence in a **** luminescence period ratio in the maintenance luminescence stroke Ic in the subfields in each which exist between them, until it succeeds in the above-mentioned selection elimination discharge within 1 field period.
[0029] Under the present circumstances, he is trying for the count by which each discharge cel changes to a nonluminescent cel from a luminescence cel to surely become 1 or less time within 1 field period, as shown in drawing 13 . That is, a luminescence drive pattern which returns again the discharge cel once set as the nonluminescent cel within 1 field period to a luminescence cel was forbidden. Therefore, since what is necessary is to carry out the above-mentioned simultaneous reset action accompanied by strong luminescence only once within 1 field period as it is shown in drawing 3 , drawing 11 , and drawing 12 in spite of not participating in image display, the fall of contrast can be suppressed.
[0030] Moreover, since the highest is also 1 time as it is shown by the black dot of drawing 13 , the selection elimination discharge carried out within 1 field period becomes possible [stopping the power consumption]. Furthermore, since a luminescence pattern which the period which is in a luminescence condition within 1 field period, and the period which will be in a nonluminescent condition reverse does not exist as shown in drawing 13 , false coutour can be controlled.
[0031] Moreover, about the above-mentioned scan pulse SP, the pulse width is more greatly set up by the subfield located in front in time of the order of subfields SF1-SF14. This is for the following reasons. Priming particle with the subfield sufficient (when it is high brightness) in discharge space when maintenance electroluminescence is fully repeated in the state of luminescence before the subfield where selection elimination actuation is performed exists, and selection elimination discharge is ensured. On the other hand, in front of the subfield where selection elimination actuation is performed, there is no subfield which will be in a luminescence condition, or the subfield which will be in a luminescence condition is, in being few, there are few counts of maintenance electroluminescence (when it is the low brightness in which selection elimination discharge is performed in the subfields [SF / SF and / 2] 1), and priming particle sufficient in discharge space does not exist. Thus, if the subfield of selection elimination actuation is greeted in the condition that priming particle sufficient in discharge space does not exist, after impressing the scan pulse SP before selection elimination discharge actually breaks out, time delay arises, and selection elimination discharge will become unstable, it will be generated in discharge in a maintenance conducting period as a result, and display quality will fall. Then, the subfield located in front in time of the order of subfields SF1-SF14 in the pulse width of the scan pulse SP is large. Namely, the subfield SF 2 (subfield of the 2nd group) which follows a subfield SF 1 in the pulse width of the scan pulse SP in the subfield SF 1 (subfield of the 1st group) of the head within 1 field period By setting up more greatly than the pulse width of a subfield SF 3 (subfield of the 3rd group), ..., the scan pulse SP in a subfield SF 14 (subfield of the 14th group) Since selection elimination discharge can surely break out during impression of the scan pulse SP, the stability of selection elimination actuation is securable.
[0032] Moreover, the pulse width of the scan pulse SP of each same subfield is set up so that the direction of the 2nd mode may serve as size from the 1st mode. This is for the following reasons. As mentioned above, according to the average intensity level of the input pixel data D, either the 1st mode and the 2nd mode are chosen, and when changing the count of luminescence of the maintenance conducting period in each same subfield (maintenance pulse number) and performing brightness control,

if the average intensity level of the input pixel data D becomes beyond a predetermined value, it will switch to the 2nd mode. In this 2nd mode, in order that the count of the maintenance electroluminescence in each same subfield may decrease as compared with the 1st mode, the priming particle excited by maintenance electroluminescence in discharge space as compared with the 1st mode decreases, the selection elimination discharge in a pixel data write-in stroke becomes unstable, discharge arises in a maintenance conducting period as a result, and display quality deteriorates. Then, by what (that is, the scanning rate of the scan pulse SP becomes long) the pulse width of the scan pulse SP of each subfield in the 2nd mode is set up for for a long time than the 1st mode, during the impression period of a scan pulse, as selection elimination discharge surely broke out, it has secured the stability of selection elimination actuation.

[0033] Moreover, pulse width of the scan pulse SP may not be changed, but you may set up so that the subfield where the pulse voltage of the scan pulse SP is located in front in time of the order of subfields SF1-SF14 may become large. That is, the pulse-voltage value of the scan pulse SP in the subfield SF 1 (subfield of the 1st group) of the head within 1 field period may be set up more greatly than the subfield SF 2 (subfield of the 2nd group) following a subfield SF 1, a subfield SF 3 (subfield of the 3rd group), ..., the pulse-voltage value of the scan pulse SP in a subfield SF 14 (subfield of the 14th group). In this case, if the pulse voltage of the scan pulse SP corresponding to subfield SF 1 - SF14 each is set to Va1-Va14 as shown in drawing 14 in the 1st mode Va1>Va2>Va3>Va4> ..... As there is relation like >Va12>Va13>Va14 and it is shown in drawing 15 in the 2nd mode When the pulse voltage of the scan pulse SP corresponding to subfield SF 1 - SF14 each is set to Vb1-Vb14, it is Vb1>Vb2>Vb3>Vb4>..... There is relation like >Vb12>Vb13>Vb14. Since the voltage level of the scan pulse SP becomes higher than the voltage level of a next subfield in time even if it is the subfields [SF / SF or / 2] 1 by this, selection elimination discharge can surely break out. Furthermore, the thing in the 2nd mode of the pulse width of the scan pulse SP of each same subfield is size from the 1st mode. That is, there are Vb1>Va1, Vb2>Va2, Vb3>Va3, ..., relation like Vb13>Va13 and Vb14>Va14. Thereby, also in the 2nd mode, selection elimination discharge can surely break out during impression of the scan pulse SP.

[0034] Furthermore, you may set up so that the subfield where both the pulse width of the scan pulse SP and a pulse voltage are located in front in time of the order of subfields SF1-SF14 may become large. Moreover, the pulse width and the pulse voltage of a scan pulse of each subfield in the subfield group which consists of subfields SF1-SF14 For example
Ta1=Ta2=Ta3=Ta4>Ta5=Ta6=Ta7=Ta8>Ta9=Ta10=Ta11=Ta12=Ta13=Ta14, You may set up like Va1=Va2=Va3=Va4>Va5=Va6=Va7=Va8>Va9=Va10=Va11=Va12=Va13=Va14.

[0035] In this case, each subfield in the subfield group which consists of SF1-SF14 With the pulse shape of the scan pulse SP in each subfield, two or more groups, Namely, the 1st group which includes at least the subfield of the head which consists of SF1-SF4, It is divided into the 2nd group which consists of SF5-SF8, and the 3rd group which consists of SF9-SF14. It is set up so that at least one of the pulse width of the scan pulse SP in the subfield belonging to the 1st group and the values of a pulse voltage may become size as compared with the value of ******** in the scan pulse in the subfield belonging to the 2nd and 3rd groups.

[0036] In addition, if the pulse width of the scan pulse SP of each subfield in the 2nd mode in which the count of luminescence is set up few from the 1st mode is set up for a long time than the 1st mode as it is shown in drawing 11 and drawing 12 , as a result, the period of the pixel data write-in stroke of each subfield may become long, and it may become difficult to drive all subfields within 1 field period. In this case, as shown in drawing 16 (a) and (b), the drive of a subfield breaks off on the way by deleting a predetermined subfield in the 2nd mode and decreasing the number of subfields, and it can prevent that display quality deteriorates.

[0037] Brightness mode can set a luminescence drive format of drawing 16 (a) in the 1st mode, and a luminescence drive format of drawing 16 (b) can be set in the 2nd mode. In the 1st mode, the 1 field consists of 14 subfields SF1-SF14 so that drawing 16 (a) may show, and the count of luminescence in the maintenance luminescence stroke Ic is set as 4, 12, 20, 32, 40, 52, 64, 76, 88, 100, and 112,128,140,156 in order of the subfield. On the other hand, in the 2nd mode, like drawing 16 (b), the 1

field consists of 13 subfields SF1-SF13, and the count of luminescence in the maintenance luminescence stroke Ic is set as 3, 9, 15, 24, 30, 39, 48, 57, 66, 75, 84, and 96,105 in order of the subfield. That is, in the 2nd mode, the luminescence drive in the subfield SF 14 which is a count subfield of the maximum luminescence in the 1st mode is stopped.

[0038] Drawing 17 is drawing showing the internal configuration of the many gradation-ized processing circuit 33 shown in drawing 4 . As it is shown in drawing 17 , the many gradation-ized processing circuit 33 consists of an error diffusion-process circuit 330 and a dithering circuit 350. First, the data separation circuit 331 in the error diffusion-process circuit 330 separates a part for part the error data and 6 bits of high orders for 2 bits of low order in the 8-bit conversion pixel data HDP supplied from the above-mentioned 1st data-conversion circuit 32 as an indicative data.

[0039] An adder 332 supplies the aggregate value which added and obtained a part for 2 bits of low order in the conversion pixel data HDP as these error data, the delay output from a delay circuit 334, and the multiplication output of the multiplier multiplier 335 to a delay circuit 336. A delay circuit 336 delays only the time delay D which has the same time amount as the clock period of pixel data for the aggregate value supplied from the adder 332, and is supplied to the above-mentioned multiplier multiplier 335 and a delay circuit 337 by making this into the delay addition signal AD 1, respectively.

[0040] The multiplier multiplier 335 supplies the multiplication result obtained by carrying out the multiplication of the predetermined multiplier value K1 (for example, "7/16") to the above-mentioned delay addition signal AD 1 to the above-mentioned adder 332. A delay circuit 337 is supplied to a delay circuit 338 by making into the delay addition signal AD 2 that from which only time amount delayed further (the 1 horizontal-scanning period-above-mentioned time delay Dx4) the above-mentioned delay addition signal AD 1. A delay circuit 338 is supplied to the multiplier multiplier 339 by making into the delay addition signal AD 3 that from which only the above-mentioned time delay D delayed this delay addition signal AD 2 further. Moreover, a delay circuit 338 is supplied to the multiplier multiplier 340 by making into the delay addition signal AD 4 what delayed this delay addition signal AD 2 further by the above-mentioned time amount which becomes time delay Dx2. Furthermore, a delay circuit 338 is supplied to the multiplier multiplier 341 by making into the delay addition signal AD 5 what delayed this delay addition signal AD 2 by the above-mentioned time amount which becomes time delay Dx3.

[0041] The multiplier multiplier 339 supplies the multiplication result obtained by carrying out the multiplication of the predetermined multiplier value K2 (for example, "3/16") to the above-mentioned delay addition signal AD 3 to an adder 342. The multiplier multiplier 340 supplies the multiplication result obtained by carrying out the multiplication of the predetermined multiplier value K3 (for example, "5/16") to the above-mentioned delay addition signal AD 4 to an adder 342. The multiplier multiplier 341 supplies the multiplication result obtained by carrying out the multiplication of the predetermined multiplier value K4 (for example, "1/16") to the above-mentioned delay addition signal AD 5 to an adder 342.

[0042] An adder 342 supplies the addition signal which added the multiplication result supplied from the above-mentioned multiplier multipliers 339 and 340 and 341 each, and was acquired to the above-mentioned delay circuit 334. This addition signal is delayed by the above-mentioned time amount time-delay D Becoming, and a delay circuit 334 supplies it to the above-mentioned adder 332. An adder 332 adds the above-mentioned error data (a part for 2 bits of low order in the conversion pixel data HDP), the delay output from a delay circuit 334, and the multiplication output of the multiplier multiplier 335, in this case, when there is no carry, it generates logical level "0", when there is carry, generates the carry out signal CO of logical level"1", and supplies it to an adder 333.

[0043] An adder 333 outputs what added the above-mentioned carry out signal CO to the above-mentioned indicative data (a part for 6 bits of high orders in the conversion pixel data HDP) as 6-bit error diffusion-process pixel data ED. Actuation of the error diffusion-process circuit 330 which becomes below from this configuration is explained. For example, although shown in drawing 18 , when asking for the error diffusion-process pixel data ED corresponding to the pixel G of **** PDP10 (j, k), First, the pixel G (j, k-1) on the left of this pixel G (j, k), the diagonally left pixel G (j-1, k-1) Each error data corresponding to the pixel G right above (j-1, k) and diagonally right pixel G (j-1, k+1) of each, that

is Pixel G Error data corresponding to (j, k-1) : error data: corresponding to 1 pixel [of delay addition signals AD] G (j-1, k+1) -- error data: corresponding to 3 pixel [of delay addition signals AD] G (j-1, k) -- error data: corresponding to 4 pixel [of delay addition signals AD] G (j-1, k-1) -- delay addition signal AD5 each Weighting addition is carried out with the **** predetermined multiplier values K1-K4 mentioned above. Next, let what added a part for 2 bits of low order of the conversion pixel data HDP, i.e., the error data corresponding to Pixel G (j, k), to this addition result, and added the carry out signal CO for 1 bit obtained at this time to a part for 6 bits of high orders in the conversion pixel data HDP, i.e., the indicative data corresponding to Pixel G (j, k), be the error diffusion-process pixel data ED.

[0044] The error diffusion-process circuit 330 a part for 6 bits of high orders in the conversion pixel data HDP by this configuration An indicative data, He regards a part for the 2 bits of the remaining low order as error data, and is trying to make what carried out weighting addition of the error data in the circumference pixels {G (j, k-1), G (j-1, k+1), G (j-1, k), G (j-1, k-1)} in each reflect in the above-mentioned indicative data. By this actuation, the brightness for 2 bits of low order in a original pixel {G (j, k)} is expressed by the above-mentioned circumference pixel in false, and, so, a brightness gradation expression equivalent to the pixel data for above-mentioned 8 bits is attained with the number of bits smaller than 8 bits, i.e., the indicative data for 6 bits.

[0045] In addition, if the multiplier value of this error diffusion is uniformly added to each pixel, the noise by the error diffusion pattern may be checked visually, and will spoil image quality. Then, you may make it change the multipliers K1-K4 of the error diffusion which should be assigned to four pixels of each like the case of the dither multiplier mentioned later for every field. By performing dithering to the error diffusion-process pixel data ED supplied from this error diffusion-process circuit 330, although the dithering circuit 350 maintains brightness gradation level equivalent to the 6-bit error diffusion-process pixel data ED, it generates the many gradation-ized processing pixel data DS which reduced the number of bits to 4 more bits. In addition, in this dithering, two or more adjoining pixels express one middle display level. For example, when performing the gradation display of 8 bits using pixel data of 6 bits of high orders of the 8-bit pixel data, right and left and four pixels which adjoin mutually up and down are made into 1 set, and four dither multiplier a-d which consists of mutually different multiplier values is assigned to the pixel data of each corresponding to 1 set of each of these pixels, respectively, and is added to them. According to this dithering, the combination of four different middle display level will occur in 4 pixels. Therefore, even if the number of bits of metaphor pixel data is 6 bits, 4 times of the brightness gradation level which can be expressed, i.e., the halftone display of 8 bits, become possible.

[0046] However, if the dither pattern which becomes dither multiplier a-d is uniformly added to each pixel, the noise by this dither pattern may be checked visually, and will spoil image quality. Then, he is trying to change above-mentioned dither multiplier a-d which should be assigned to four pixels of each for every field in the dithering circuit 350.

[0047] Drawing 19 is drawing showing the internal configuration of this dithering circuit 350. In drawing 19 , the dither multiplier generating circuit 352 generates four dither multipliers a, b, c, and d every four pixels which adjoins mutually, and supplies these to an adder 351 one by one. for example, the pixel G corresponding to [as shown in drawing 20] the j-th line (j, k) and Pixel G (j, k+1), the pixel G (j+1, k) corresponding to a ** (j+1) line, and pixel G (j+1, k+1) -- four dither multipliers a, b, c, and d corresponding to four pixels of each are generated. Under the present circumstances, for every field, it changes and the dither multiplier generating circuit 352 goes, as above-mentioned dither multiplier a-d which should be assigned to these four pixels of each is shown in drawing 20 .

[0048] Namely, it sets in the first field [1st]. Pixel G (j, k) : dither multiplier apixelG (j, k+1) : dither multiplier bpixelG (j+1, k) :dither multiplier cpixelG (j+1, k+1) : In the 2nd field of the d-th dither multiplier Pixel G (j, k) : dither multiplier bpixelG (j, k+1) : dither multiplier apixelG (j+1, k) :dither multiplier dpixelG (j+1, k+1) : In the 3rd field of the c-th dither multiplier pixel G (j, k) :dither multiplier dpixelG (j, k+1) :dither multiplier cpixelG (j+1, k) : -- the dither multiplier [of b pixels] G (j+1, k+1):dither multiplier a -- and It sets in the 4th field and is Pixel G (j, k). : dither multiplier cpixelG (j, k+1) : dither multiplier dpixelG (j+1, k) :dither multiplier apixelG (j+1, k+1) : In the assignment like

the dither multiplier b, circulate through dither multiplier a-d and it generates repeatedly. This is supplied to an adder 351. The dither multiplier generating circuit 352 repeats and performs actuation of the 1st field of **** mentioned above - the 4th field. That is, if dither multiplier generating actuation in this 4th field is completed, again, it will return to actuation of the 1st field of the above, and the actuation mentioned above will be repeated.

[0049] The above-mentioned pixel G to which an adder 351 is supplied from the above-mentioned error diffusion-process circuit 330 (j, k) To error diffusion-process pixel data ED of each corresponding to Pixel G (j, k+1), Pixel G (j+1, k), and pixel G (j+1, k+1) of each Like ****, dither multiplier a-d assigned for every field is added, respectively, and the dither addition pixel data obtained at this time are supplied to the high-order-bit extract circuit 353.

[0050] For example, it sets in the 1st field shown in drawing 20 . The error diffusion-process pixel data ED+ dither multiplier a corresponding to Pixel G (j, k) The error diffusion-process pixel data ED+ dither multiplier b corresponding to Pixel G (j, k+1) By using each of the error diffusion-process pixel data ED+ dither multiplier c corresponding to Pixel G (j+1, k), and the error diffusion-process pixel data ED+ dither multiplier d corresponding to Pixel G (j+1, k+1) as dither addition pixel data, sequential supply is carried out and it goes to the high-order-bit extract circuit 353.

[0051] The high-order-bit extract circuit 353 extracts even a part for 4 bits of high orders of these dither addition pixel data, and supplies it to the 2nd data-conversion circuit 34 shown in drawing 4 by making this into the many gradation-ized pixel data DS. the 1- corresponding to [although the 2nd data-conversion circuit 34 was shown in drawing 21 in these many gradation-ized pixel data DS] subfield SF 1 - SF14 each according to the **** translation table -- it changes into the conversion pixel data (display pixel data) HD which consist of the 14th bit. In addition, the many gradation-ized pixel data DS make the 8 bits (256 gradation) input pixel data D 224/225 according to the 1st data conversion (drawing 9 and translation table of drawing 10), and further, 2 bits is compressed by for example, error diffusion process and the many gradation-ized processing like dithering, respectively, and they are changed into a total of 4 bits (15 gradation) data by them.

[0052] the 1- [in / here / the conversion pixel data HD] -- the inside of the 14th bit, and logical level -- the bit of "1" shows making selection elimination discharge carry out in the pixel data write-in stroke Wc in the subfield SF corresponding to the bit. Here, the above-mentioned conversion pixel data HD corresponding to each discharge cel of PDP10 are supplied to the address driver 6 through memory 4. Under the present circumstances, although the gestalt of the conversion pixel data HD corresponding to 1 discharge cel is surely shown in drawing 21 , it is set to any 1 of the **** 15 patterns. The address driver 6 assigns the 1st in the above-mentioned conversion pixel data HD - the 14th bit of each to one to subfield SF14 each, when the bit logic is logical level "1", it is restricted, it generates the pixel data pulse of the high voltage in the pixel data write-in stroke Wc in the corresponding subfield, and impresses this to the train electrode D of PDP10. Thereby, the above-mentioned selection elimination discharge occurs.

[0053] Although the 8-bit pixel data D are changed into the 14-bit conversion pixel data HD by the data-conversion circuit 30, it is shown in drawing 21 like the above and the gradation display of 15 step of **** comes to be carried out, the gradation expression on actual vision becomes 256 gradation by actuation of the **** many gradation-ized processing circuit 33 mentioned above. The discharge which has set to the subfield of the head within 1 field period, and initializes all discharge cels with a chisel first in the condition of a luminescence cel (when the selection elimination address method is adopted) or a nonluminescent cel (when a selection write-address method is adopted) is made to occur like the above by the drive approach shown in drawing 3 - drawing 21 . Next, it has set in the pixel data write-in stroke in any 1 subfield, and each discharge cel is set as a nonluminescent cel or a luminescence cel with a chisel according to pixel data. Furthermore, he is trying only for the luminescence period corresponding to weighting of a subfield to make only the above-mentioned luminescence cel emit light in the luminescence maintenance stroke in each subfield. According to this drive approach, along with the increment in the brightness which should be displayed in the case of the selection elimination address method, it will be in a luminescence condition from the subfield of the head of the 1 field at

order, and, on the other hand, will be in a luminescence condition from the subfield at the tail end of the 1 field at order along with the increment in the brightness which should be displayed in the case of the selection elimination address method.
[0054] In addition, in the above-mentioned example, although the halftone expression of 15 gradation is performed by making into 1 time the simultaneous reset action carried out within 1 field period, it is also possible to increase the number of gradation by performing the starting simultaneous reset action twice. Drawing 22 is drawing showing the luminescence drive format in which it succeeded in view of this point.
[0055] In addition, drawing 22 shows the luminescence drive format applied when the **** selection elimination address method mentioned above as a pixel data write-in approach is adopted. In the luminescence drive format shown in drawing 22 , 1 field period was divided into 14 subfields which consist of subfields SF1-SF14, and these are further divided into the subfield group which consists of subfields SF1-SF6, and the subfield group which consists of subfields SF7-SF14. In each subfield, the pixel data write-in stroke Wc which writes in pixel data and performs a setup of a luminescence cel and a nonluminescent cel, and the maintenance luminescence stroke Ic which maintains a luminescence condition only to a luminescence cel are carried out. Under the present circumstances, the luminescence period (count of luminescence) in each maintenance luminescence stroke Ic is set as SF1:1SF2:1SF3:1SF4:3SF5:3SF6:8SF7:13SF8:15SF9:20SF10:25SF11:31SF12:37SF13:48SF14:50, when the count ratio of luminescence in a subfield SF 1 is set to "1."
[0056] That is, it is non-linearity (namely, a reverse gamma ratio, Y=X2.2) about the ratio of the count of luminescence of each subfields SF1-SF14. It sets up so that it may change, and he is trying for this to amend the nonlinear characteristic (gamma property) of the input pixel data D. Furthermore, as shown in drawing 22 , the elimination stroke E which makes the wall charge which performs the simultaneous reset stroke Rc only in the subfields SF1 and SF7 of the head in each subfield group, and remains in all discharge cels only in the subfields SF6 and SF14 at the tail end in each subfield group disappear is performed.
[0057] Also in the luminescence drive format shown in drawing 22 the pulse width and/or the pulse voltage of the scan pulse SP Each subfield groups SF1-SF6 and the subfield located in front in time in SF7-SF14 set up more greatly, And setting the pulse width and/or the pulse voltage of the scan pulse SP of each same subfield as size as compared with the 1st mode in the 2nd mode in which the count of luminescence is set up few, from the 1st mode is performed.
[0058] In addition, the count of luminescence of each subfields SF1-SF14 in the 1st mode is set as 4, 4, 4, 12, 12, 32, 52, 60, 80, 100, and 124,148,192,200 in order of a subfield, for example, and the count of luminescence of each subfields SF1-SF14 in the 2nd mode is set as 3, 3, 3, 9, 9, 24, 39, 45, 60, 75, and 93,111,144,150 in order of a subfield.
[0059] In case drawing 23 and drawing 24 perform the luminescence drive based on the luminescence drive format shown in drawing 22 , they are drawing showing an example of the translation table used in the 1st data-conversion circuit 32 shown in drawing 4 . The 1st data-conversion circuit 32 is changed into the 9 bits (0-352) conversion pixel data HDp which set the input brilliance-control pixel data DBL of 256 gradation (eight pits) to 22x16 / 255 (352/255) based on the translation table of drawing 23 and drawing 24 , and is supplied to the many gradation-ized processing circuit 33. In the many gradation-ized processing circuit 33, compression processing for 4 bits is performed like ****, and the 5 bits (0-22) many gradation-ized pixel data Ds are outputted.
[0060] Under the present circumstances, although the 2nd data-conversion circuit 34 shown in drawing 4 is shown in drawing 2525 , it changes these 5-bit many gradation-ized pixel data DS according to a **** translation table, and it obtains the 14-bit conversion pixel data (display pixel data) HD. Under the present circumstances, drawing 25 is drawing showing the translation table of the 2nd data-conversion circuit 34 used when the describing [above] selection elimination address method is adopted as a pixel data writing-in method, and all the patterns of a luminescence drive, respectively.
[0061] thus, although shown in drawing 22 - drawing 25 , if a **** drive is carried out, it is shown also in drawing 25 -- as -- a luminescence brightness ratio -- {0, 1, 2, 3, 6, 9, 17, 22, 30, 37, 45, 57, 65, 82,

90, 113, 121, 150, 158, 195, 206, 245, 256}
23 steps of becoming halftone expressions are attained.
[0062] Like the above, the subfield within 1 field period is divided into two subfield groups which consist of two or more subfields arranged continuously mutually by the drive approach shown in drawing 22 - drawing 25 . When the selection elimination address method is adopted, as shown in drawing 22 , it divides into the subfield group which consists of subfields SF1-SF6, and the subfield group which consists of SF7-SF14. Under the present circumstances, it has set to the subfield of the head of each subfield group, the simultaneous reset stroke Rc is performed with a chisel, respectively, and the discharge which initializes all discharge cels in the condition of a luminescence cel is made to occur. Here, it has set in the write-in stroke of the pixel data of any 1 subfield in each subfield group, and a discharge cel is set as a nonluminescent cel or a luminescence cel with a chisel according to pixel data. Furthermore, he is trying only for the luminescence period corresponding to weighting of a subfield to make only the above-mentioned luminescence cel emit light in the luminescence maintenance stroke in each subfield. Therefore, simultaneous reset action and selection elimination actuation becomes 1 time each in each subfield group. According to this drive approach, it takes to the increment in the brightness which should be displayed in the case of the selection elimination address method, and will be in a luminescence condition from the subfield of the head in each subfield group at order.
[0063] in addition, by the drive approach shown in drawing 3 mentioned above - drawing 21 By the pixel data write-in stroke Wc of any 1 of the subfield groups SF1-SF14, and the drive approach shown in drawing 22 - drawing 25 he carries out coincidence impression of the scan pulse SP and the pixel data pulse of the high voltage, and is trying to make selection elimination discharge occur in the subfield groups SF1-SF6 and the pixel data write-in stroke Wc of any 1 of SF7-SF14 each
[0064] However, if there are few amounts of the charged particle which remains in a discharge cel, even if these scan pulse SP and the pixel data pulse of the high voltage are impressed to coincidence, selection elimination discharge may be unable to eliminate wall charge in a discharge cel, without occurring normally. By the drive approach shown in drawing 21 in this case, for example, drawing 3 , -, even if the pixel data D after A/D conversion are data in which low brightness is shown, it will succeed in luminescence corresponding to the highest brightness, and the problem of reducing image quality remarkably arises.
[0065] For example, when the selection elimination address method is adopted as a pixel data writing-in method, the conversion pixel data HD are [01000000000000].
As it comes out and is shown by the black dot of drawing 21 in a certain case, it has set to the subfield SF 2, selection elimination discharge is carried out with a chisel, and a discharge cel changes to a nonluminescent cel in this case. Thereby, it has set in SF1 of the subfields SF1-SF14, and maintenance luminescence should be carried out with the chisel. However, if it means that selection elimination in this subfield SF 2 went wrong, and wall charge remained with as in this discharge cel, maintenance luminescence will be carried out also not only in the subfield SF 1 but in the subfields SF2-SF14 after it, and it will succeed in the highest brightness display as a result.
[0066] Then, in this invention, in order to raise further the stability of the selection elimination actuation in the drive approach of drawing 3 - drawing 21 or drawing 22 - drawing 25 , although shown in drawing 26 - drawing 29 , a **** luminescence drive pattern is adopted, and the luminescence actuation which made the mistake in being such is prevented certainly. In case drawing 26 - drawing 29 carry out the luminescence drive pattern in which it succeeded that the luminescence actuation which made the mistake in being such should be prevented, and this luminescence drive, they are drawing showing an example of the translation table used in the 2nd data-conversion circuit 34.
[0067] Under the present circumstances, in carrying out this luminescence drive in all the patterns of the luminescence drive performed based on a **** luminescence drive format, and a list, although shown in drawing 3 which has established the simultaneous reset stroke Rc only once during 1 field period, by drawing 26 - drawing 28 , an example of the translation table used in the 2nd data-conversion circuit 34 is shown, respectively. In addition, although drawing 26 - drawing 28 are shown in drawing 3 , they

show the pattern of the luminescence drive performed based on the luminescence drive format at the time of adopting the **** selection elimination address method, respectively.
[0068] Moreover, by drawing 29 , although shown in drawing 22 which has established the simultaneous reset stroke Rc twice during 1 field period, in case this luminescence drive is carried out in all the patterns of the luminescence drive performed based on a **** luminescence drive format, and a list, an example of the translation table used in the 2nd data-conversion circuit 34 is shown, respectively. by the luminescence drive pattern shown in **** drawing 26 or drawing 29 mentioned above, as shown in the black dot in drawing, it is made to carry out selection elimination discharge here in two pixel data [of each subfield] write-in strokes Wc which continued mutually continuously.
[0069] Since according to this actuation disappearance of wall charge is normally performed by the 2nd selection elimination discharge even if it can compare and cannot extinguish wall charge in a discharge cel normally by the 1st selection elimination discharge, ********** maintenance luminescence mentioned above is prevented. In addition, it is not necessary to perform selection elimination discharge of these 2 batch in the subfield which continued mutually. In short, what is necessary is just made to perform 2nd selection elimination discharge in one of the subfields after the 1st selection elimination discharge is completed.
[0070] Drawing 27 is drawing showing an example of the translation table of the luminescence drive pattern in which it succeeded in view of this point, and the 2nd data-conversion circuit 34. In an example shown in drawing 27 , as shown in the black dot in drawing, it is made to perform 2nd selection elimination discharge from 1 subfield ****** after the 1st implementation of selection elimination discharge.
[0071] Moreover, the count of the selection elimination discharge carried out within 1 field period is not limited to 2 times. Drawing 28 R> 8 is drawing showing an example of the translation table of the luminescence drive pattern in which it succeeded in view of this point, and the 2nd data-conversion circuit 34. In addition, it is shown that any of "* "logical level" 1" or "0" which are shown in drawing 28 are sufficient, and the trigonum mark shows that it restricts when it is "* "logical level" 1" starting, and selection elimination discharge is performed.
[0072] Since there is a possibility that the store of pixel data may go wrong, by first-time selection elimination discharge in short, it is at least one of the subfields which exist after it, and the store of pixel data is again ensured by performing selection elimination discharge.
[0073]
[Effect of the Invention] As explained in full detail above, in the drive approach of the plasma display of this invention, although false coutour is controlled, improvement in contrast can be aimed at with a low power, selection discharge can be stabilized further, and improvement in display quality can be aimed at.

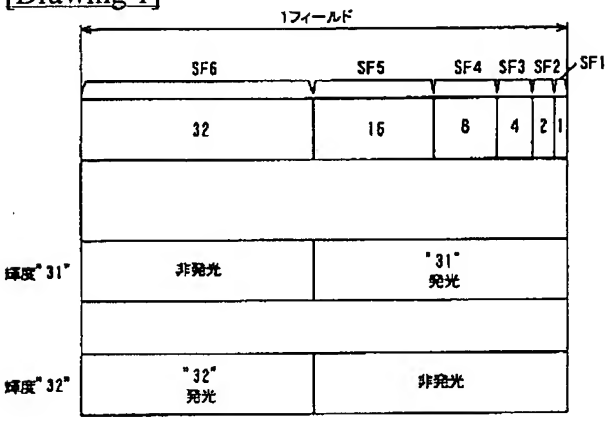
[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

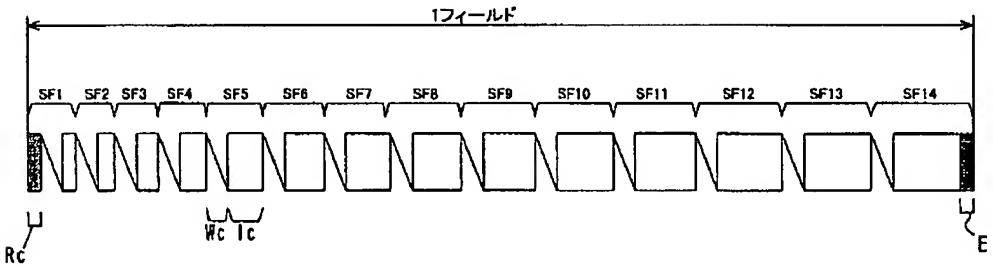
DRAWINGS

[Drawing 1]

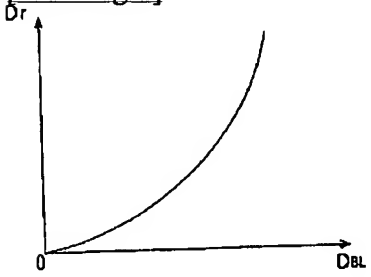


[Drawing 3]

【選択消去】



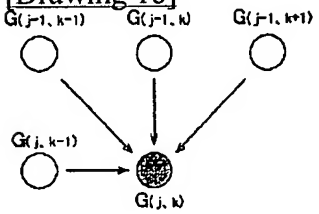
[Drawing 6]



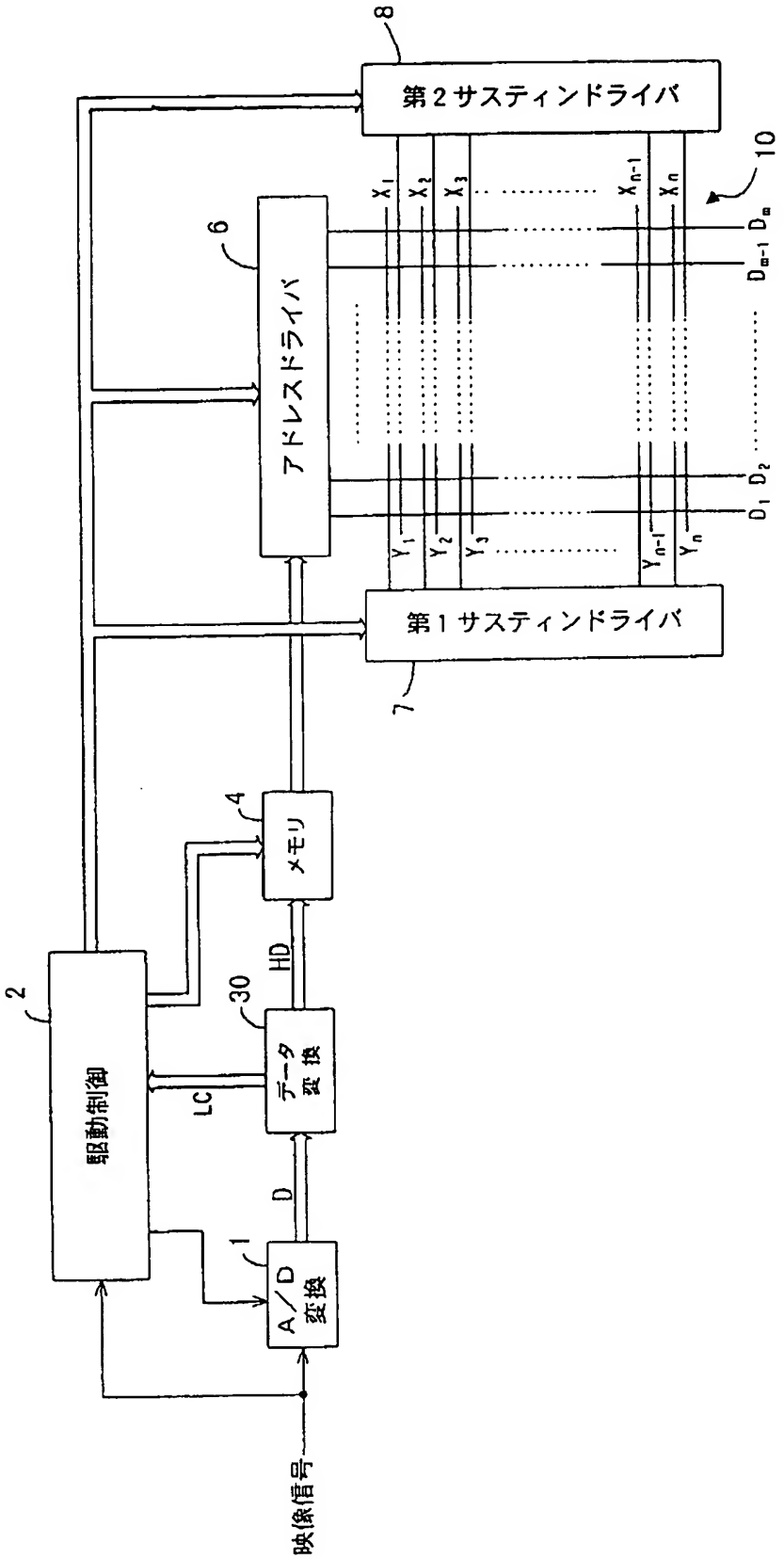
[Drawing 7]

LC	SF1	SF2	SF3	SF4	SF5	SF6	SF7	SF8	SF9	SF10	SF11	SF12	SF13	SF14
第1モード	4	12	20	32	40	52	64	76	88	100	112	128	140	156
第2モード	3	9	15	24	30	39	48	57	66	75	84	96	105	117

[Drawing 18]

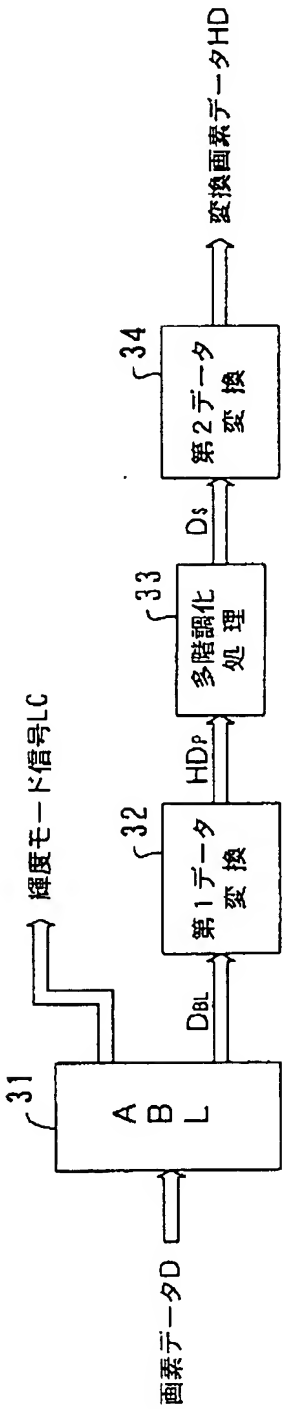


[Drawing 2]


8
第2サスティンドライバ
10
X1 X2 X3 ..... Xn-1 Xn
6
アドレスドライバ
Dm Dm-1 ..... D2 D1
Y1 Y2 Y3 ..... Yn-1 Yn
第1サスティンドライバ
7
4
メモリ
HD
30
データ変換
LC
2
駆動制御
D
1
A/D変換
映像信号

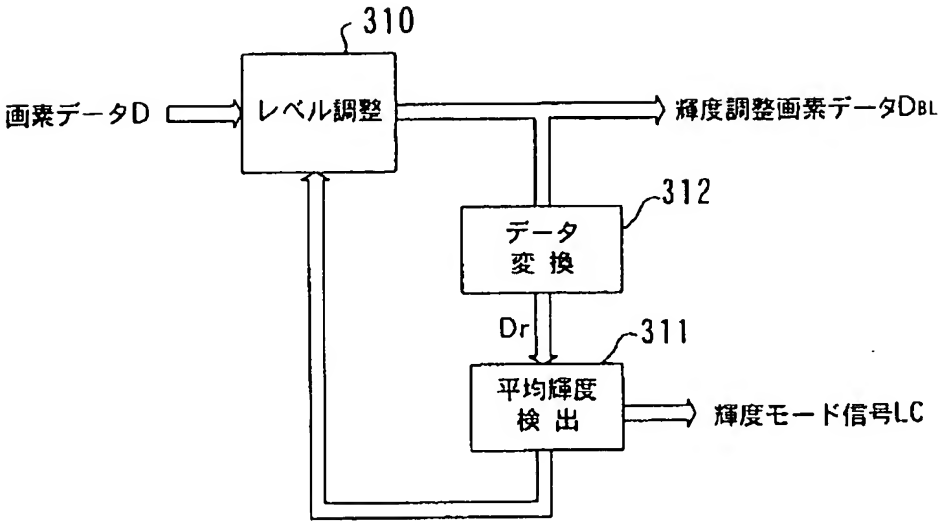
[Drawing 4]

30

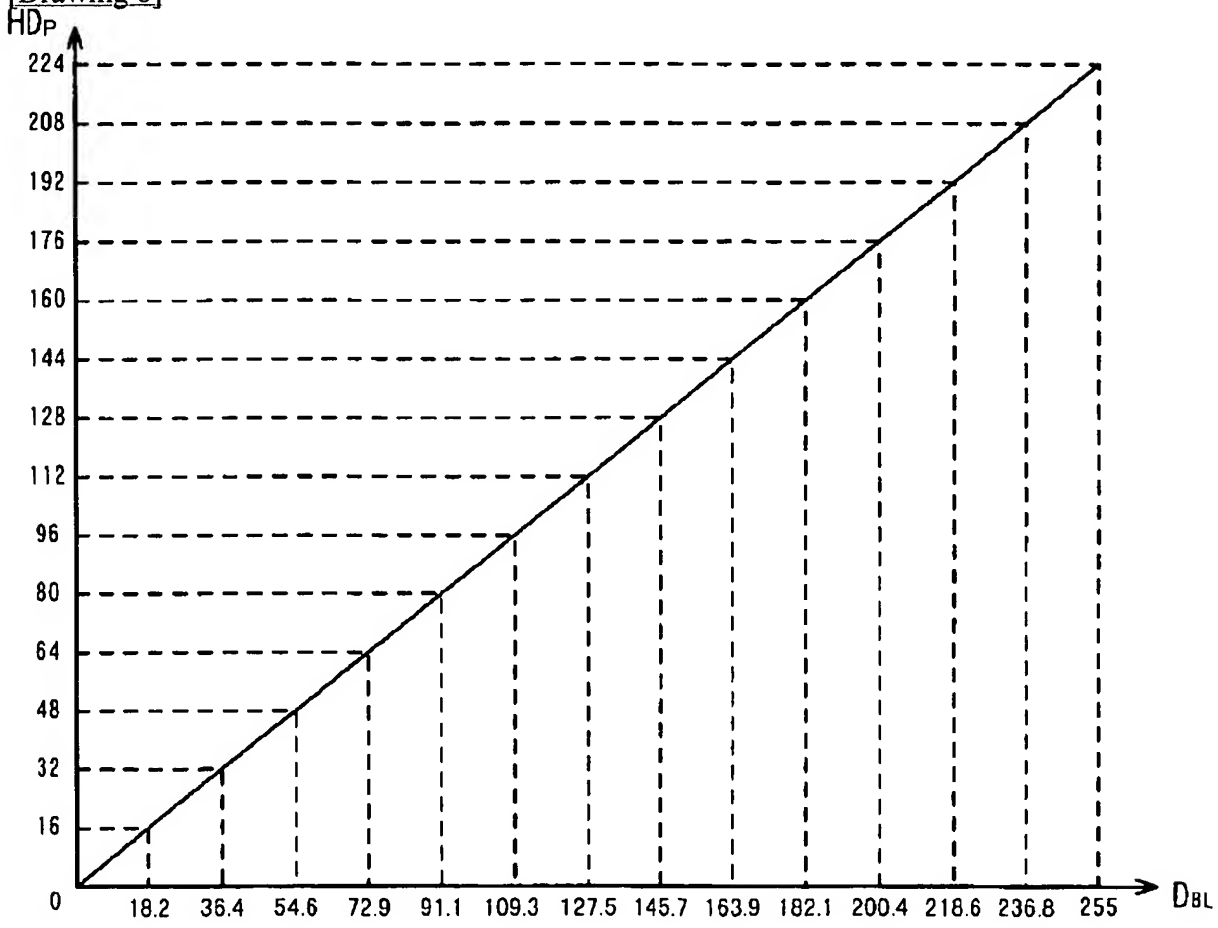

画素データD
31
ABL
輝度モード信号LC
DBL
32
第1データ変換
HDP
33
多階調化処理
DS
34
第2データ変換
変換画素データHD

[Drawing 5]

31



[Drawing 8]



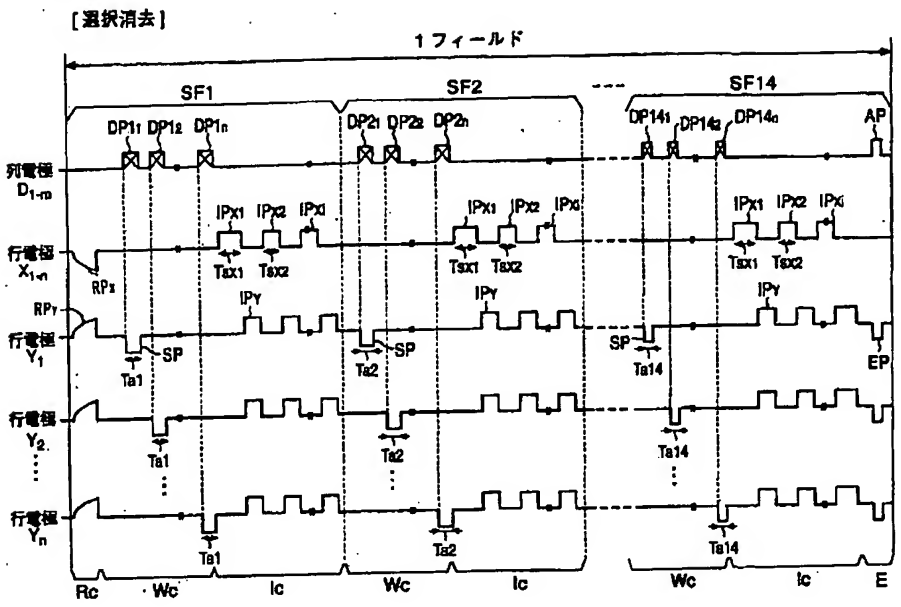
[Drawing 9]

D_{BL}		HD_P		D_{BL}		HD_P	
輝度	0～7	輝度	0～7	輝度	0～7	輝度	0～7
0	00000000	0	00000000	64	01000000	56	00111000
1	00000001	0	00000000	65	01000001	57	00111001
2	00000010	1	00000001	66	01000010	57	00111001
3	00000011	2	00000010	67	01000011	58	00111010
4	00000100	3	00000011	68	01000100	59	00111011
5	00000101	4	00000100	69	01000101	60	00111100
6	00000110	5	00000101	70	01000110	61	00111101
7	00000111	6	00000110	71	01000111	62	00111110
8	00001000	7	00000111	72	01001000	63	00111111
9	00001001	7	00000111	73	01001001	64	01000000
10	00001010	8	00001000	74	01001010	65	01000001
11	00001011	9	00001001	75	01001011	65	01000001
12	00001100	10	00001010	76	01001100	66	01000010
13	00001101	11	00001011	77	01001101	67	01000011
14	00001110	12	00001100	78	01001110	68	01000100
15	00001111	13	00001101	79	01001111	69	01000101
16	00010000	14	00001110	80	01010000	70	01000110
17	00010001	14	00001110	81	01010001	71	01000111
18	00010010	15	00001111	82	01010010	72	01001000
19	00010011	16	00010000	83	01010011	72	01001000
20	00010100	17	00010001	84	01010100	73	01001001
21	00010101	18	00010010	85	01010101	74	01001010
22	00010110	19	00010011	86	01010110	75	01001011
23	00010111	20	00010100	87	01010111	76	01001100
24	00011000	21	00010101	88	01011000	77	01001101
25	00011001	21	00010101	89	01011001	77	01001101
26	00011010	22	00010110	90	01011010	78	01001110
27	00011011	23	00010111	91	01011011	79	01001111
28	00011100	24	00011000	92	01011100	80	01010000
29	00011101	25	00011001	93	01011101	81	01010001
30	00011110	26	00011010	94	01011110	82	01010010
31	00011111	27	00011011	95	01011111	83	01010011
32	00100000	28	00011100	96	01100000	84	01010100
33	00100001	28	00011100	97	01100001	85	01010101
34	00100010	29	00011101	98	01100010	86	01010110
35	00100011	30	00011110	99	01100011	86	01010110
36	00100100	31	00011111	100	01100100	87	01010111
37	00100101	32	00100000	101	01100101	88	01011000
38	00100110	33	00100001	102	01100110	89	01011001
39	00100111	34	00100010	103	01100111	90	01011010
40	00101000	35	00100011	104	01101000	91	01011011
41	00101001	36	00100100	105	01101001	92	01011100
42	00101010	36	00100100	106	01101010	93	01011101
43	00101011	37	00100101	107	01101011	93	01011101
44	00101100	38	00100110	108	01101100	94	01011110
45	00101101	39	00100111	109	01101101	95	01011111
46	00101110	40	00101000	110	01101110	96	01100000
47	00101111	41	00101001	111	01101111	97	01100001
48	00110000	42	00101010	112	01110000	98	01100010
49	00110001	43	00101011	113	01110001	99	01100011
50	00110010	43	00101011	114	01110010	100	01100100
51	00110011	44	00101100	115	01110011	101	01100101
52	00110100	45	00101101	116	01110100	101	01100101
53	00110101	46	00101110	117	01110101	102	01100110
54	00110110	47	00101111	118	01110110	103	01100111
55	00110111	48	00110000	119	01110111	104	01101000
56	00111000	49	00110001	120	01111000	105	01101001
57	00111001	50	00110010	121	01111001	106	01101010
58	00111010	50	00110010	122	01111010	107	01101011
59	00111011	51	00110011	123	01111011	108	01101100
60	00111100	52	00110100	124	01111100	108	01101100
61	00111101	53	00110101	125	01111101	109	01101101
62	00111110	54	00110110	126	01111110	110	01101110
63	00111111	55	00110111	127	01111111	111	01101111

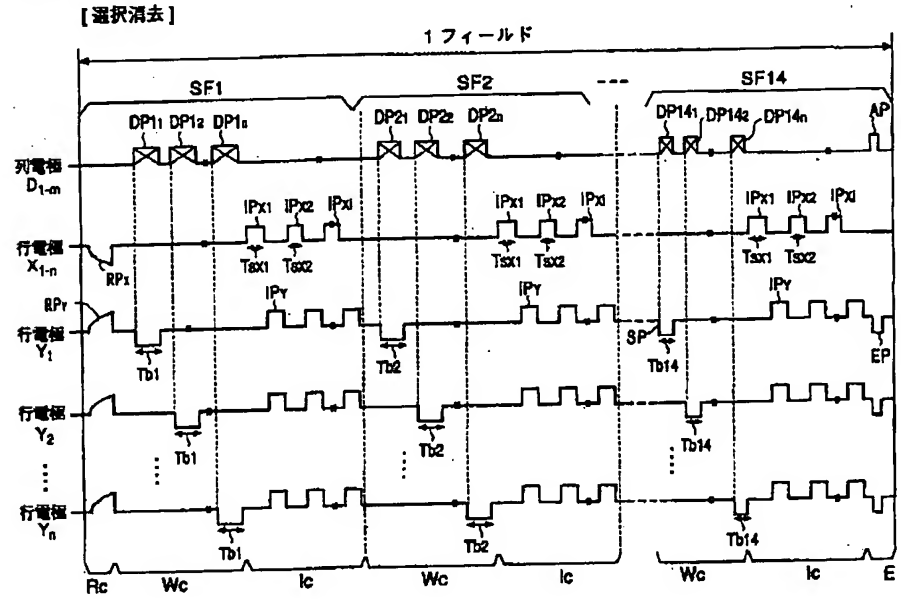
[Drawing 10]

D_{BL}		HD_P		D_{BL}		HD_P	
輝度	0 ～ 7	輝度	0 ～ 7	輝度	0 ～ 7	輝度	0 ～ 7
128	10000000	112	01110000	192	11000000	168	10101000
129	10000001	113	01110001	193	11000001	169	10101001
130	10000010	114	01110010	194	11000010	170	10101010
131	10000011	115	01110011	195	11000011	171	10101011
132	10000100	115	01110011	196	11000100	172	10101100
133	10000101	116	01110100	197	11000101	173	10101101
134	10000110	117	01110101	198	11000110	173	10101101
135	10000111	118	01110110	199	11000111	174	10101110
136	10001000	119	01110111	200	11001000	175	10101111
137	10001001	120	01111000	201	11001001	176	10110000
138	10001010	121	01111001	202	11001010	177	10110001
139	10001011	122	01111010	203	11001011	178	10110010
140	10001100	122	01111010	204	11001100	179	10110011
141	10001101	123	01111011	205	11001101	180	10110100
142	10001110	124	01111100	206	11001110	180	10110100
143	10001111	125	01111101	207	11001111	181	10110101
144	10010000	126	01111110	208	11010000	182	10110110
145	10010001	127	01111111	209	11010001	183	10110111
146	10010010	128	10000000	210	11010010	184	10111000
147	10010011	129	10000001	211	11010011	185	10111001
148	10010100	130	10000010	212	11010100	186	10111010
149	10010101	130	10000010	213	11010101	187	10111011
150	10010110	131	10000011	214	11010110	187	10111011
151	10010111	132	10000100	215	11010111	188	10111100
152	10011000	133	10000101	216	11011000	189	10111101
153	10011001	134	10000110	217	11011001	190	10111110
154	10011010	135	10000111	218	11011010	191	10111111
155	10011011	136	10001000	219	11011011	192	11000000
156	10011100	137	10001001	220	11011100	193	11000001
157	10011101	137	10001001	221	11011101	194	11000010
158	10011110	138	10001010	222	11011110	195	11000011
159	10011111	139	10001011	223	11011111	195	11000011
160	10100000	140	10001100	224	11100000	196	11000100
161	10100001	141	10001101	225	11100001	197	11000101
162	10100010	142	10001110	226	11100010	198	11000110
163	10100011	143	10001111	227	11100011	199	11000111
164	10100100	144	10010000	228	11100100	200	11001000
165	10100101	144	10010000	229	11100101	201	11001001
166	10100110	145	10010001	230	11100110	202	11001010
167	10100111	146	10010010	231	11100111	202	11001010
168	10101000	147	10010011	232	11101000	203	11001011
169	10101001	148	10010100	233	11101001	204	11001100
170	10101010	149	10010101	234	11101010	205	11001101
171	10101011	150	10010110	235	11101011	206	11001110
172	10101100	151	10010111	236	01101100	207	11001111
173	10101101	151	10010111	237	11101101	208	11010000
174	10101110	152	10011000	238	11101110	209	11010001
175	10101111	153	10011001	239	11101111	209	11010001
176	10110000	154	10011010	240	11110000	210	11010010
177	10110001	155	10011011	241	11110001	211	11010011
178	10110010	156	10011100	242	11110010	212	11010100
179	10110011	157	10011101	243	11110011	213	11010101
180	10110100	158	10011110	244	11110100	214	11010110
181	10110101	158	10011110	245	11110101	215	11010111
182	10110110	159	10011111	246	11110110	216	11011000
183	10110111	160	10100000	247	11110111	216	11011001
184	10111000	161	10100001	248	11111000	217	11011010
185	10111001	162	10100010	249	11111001	218	11011010
186	10111010	163	10100011	250	11111010	219	11011011
187	10111011	164	10100100	251	11111011	220	11011100
188	10111100	165	10100101	252	11111100	221	11011101
189	10111101	166	10100110	253	11111101	222	11011110
190	10111110	166	10100110	254	11111110	223	11011111
191	10111111	167	10100111	255	11111111	224	11100000

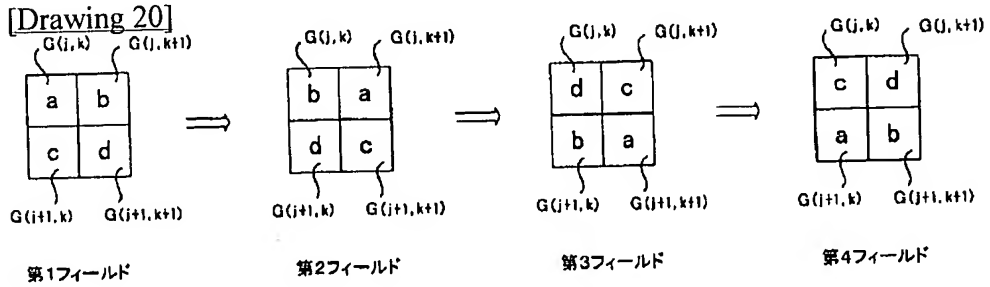
[Drawing 11]



[Drawing 12]



[Drawing 20]



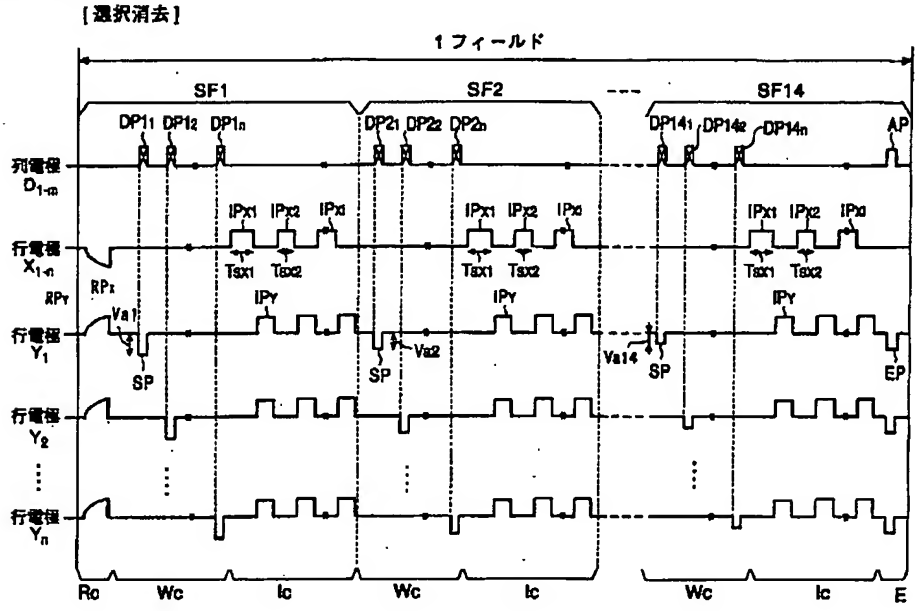
[Drawing 13]

[選択消去]

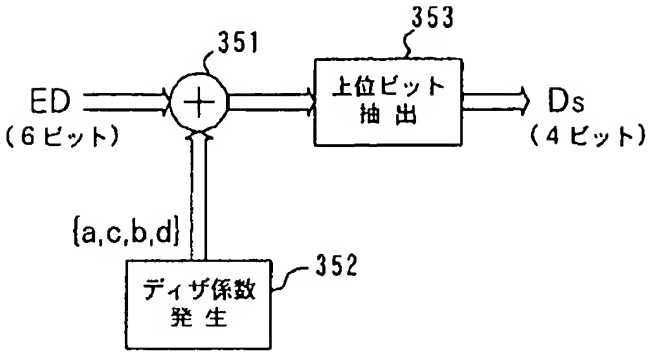
階調	SF1	SF2	SF3	SF4	SF5	SF6	SF7	SF8	SF9	SF10	SF11	SF12	SF13	SF14	発光輝度 第1モード	発光輝度 第2モード
1	●														0	0
2	○	●													4	3
3	○	○	●												16	12
4	○	○	○	●											36	27
5	○	○	○	○	●										68	51
6	○	○	○	○	○	●									108	81
7	○	○	○	○	○	○	●								160	120
8	○	○	○	○	○	○	○	●							224	168
9	○	○	○	○	○	○	○	○	●						300	225
10	○	○	○	○	○	○	○	○	○	●					388	291
11	○	○	○	○	○	○	○	○	○	○	●				488	366
12	○	○	○	○	○	○	○	○	○	○	○	●			600	450
13	○	○	○	○	○	○	○	○	○	○	○	○	●		728	546
14	○	○	○	○	○	○	○	○	○	○	○	○	○	●	868	651
15	○	○	○	○	○	○	○	○	○	○	○	○	○	○	1024	768

黒丸:選択消去放電
白丸:発光

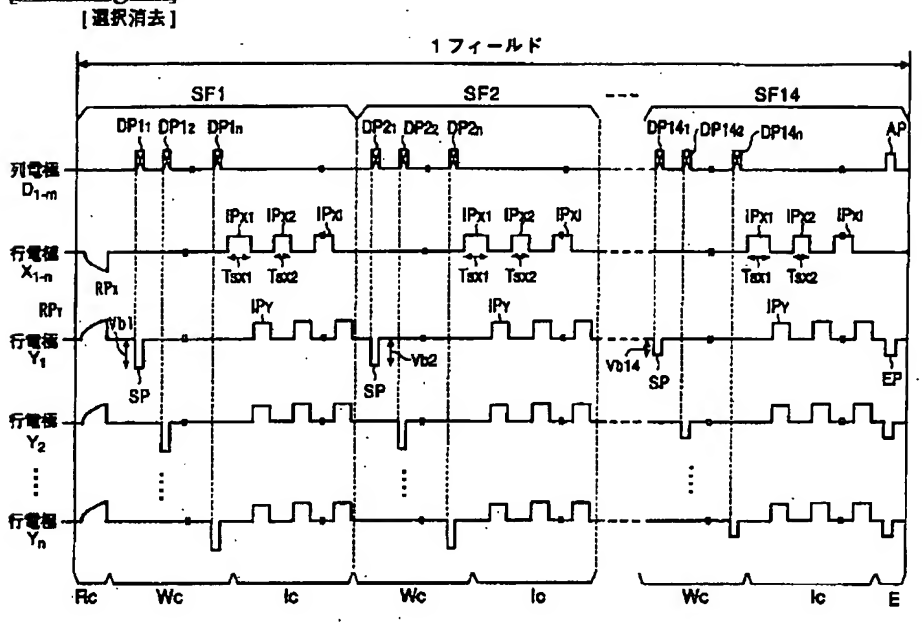
[Drawing 14]



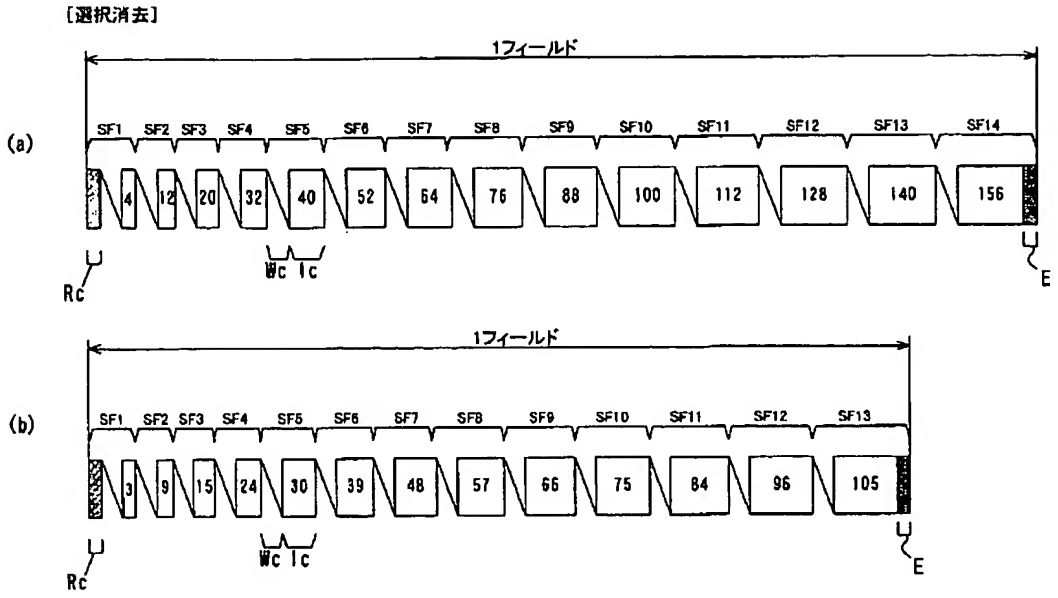
[Drawing 19]



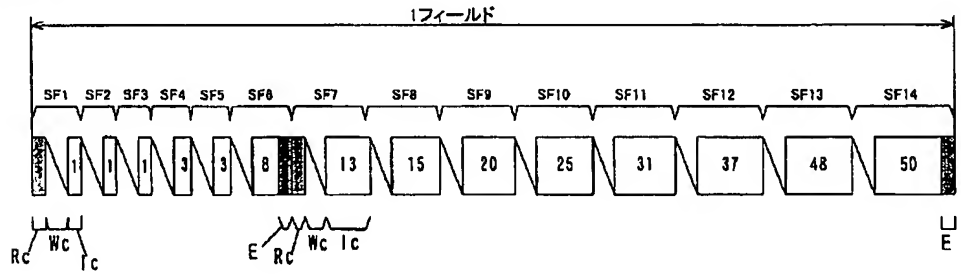
[Drawing 15]



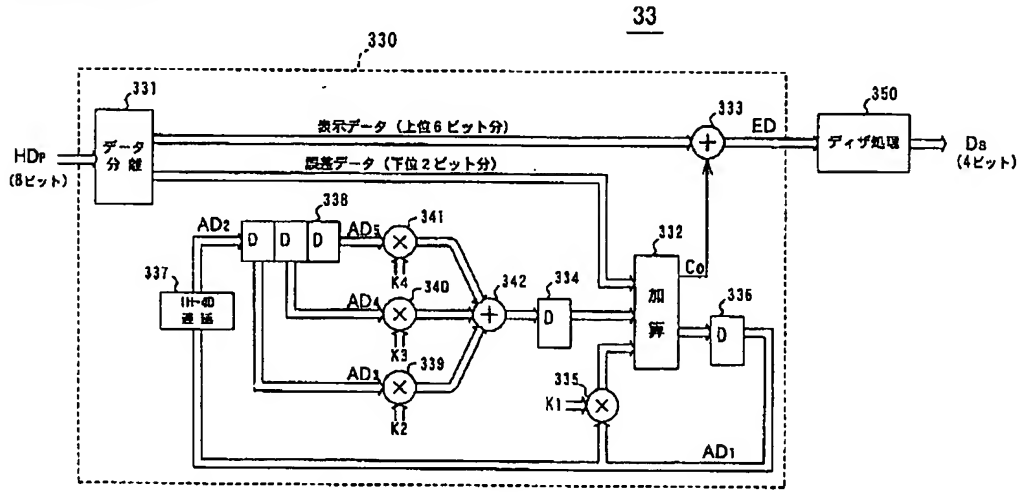
[Drawing 16]



[Drawing 22]



[Drawing 17]



[Drawing 21]

[選択消去]

Ds	HD														1フィールドにおける発光駆動パターン														発光輝度
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	SF 1	SF 2	SF 3	SF 4	SF 5	SF 6	SF 7	SF 8	SF 9	SF 10	SF 11	SF 12	SF 13	SF 14	
0000	1	0	0	0	0	0	0	0	0	0	0	0	0	0	●														0
0001	0	1	0	0	0	0	0	0	0	0	0	0	0	0	○	●													1
0010	0	0	1	0	0	0	0	0	0	0	0	0	0	0	○	○	●												4
0011	0	0	0	1	0	0	0	0	0	0	0	0	0	0	○	○	○	●											9
0100	0	0	0	0	1	0	0	0	0	0	0	0	0	0	○	○	○	○	●										17
0101	0	0	0	0	0	1	0	0	0	0	0	0	0	0	○	○	○	○	○	●									27
0110	0	0	0	0	0	0	1	0	0	0	0	0	0	0	○	○	○	○	○	○	●								40
0111	0	0	0	0	0	0	0	1	0	0	0	0	0	0	○	○	○	○	○	○	○	●							56
1000	0	0	0	0	0	0	0	0	1	0	0	0	0	0	○	○	○	○	○	○	○	○	●						75
1001	0	0	0	0	0	0	0	0	0	1	0	0	0	0	○	○	○	○	○	○	○	○	○	●					97
1010	0	0	0	0	0	0	0	0	0	0	1	0	0	0	○	○	○	○	○	○	○	○	○	○	●				122
1011	0	0	0	0	0	0	0	0	0	0	0	1	0	0	○	○	○	○	○	○	○	○	○	○	○	●			150
1100	0	0	0	0	0	0	0	0	0	0	0	0	1	0	○	○	○	○	○	○	○	○	○	○	○	○	●		182
1101	0	0	0	0	0	0	0	0	0	0	0	0	0	1	○	○	○	○	○	○	○	○	○	○	○	○	○	●	217
1110	0	0	0	0	0	0	0	0	0	0	0	0	0	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	256

黒丸:選択消去放電
白丸:発光

[Drawing 23]

D_{BL}		HD_P		D_{BL}		HD_P	
輝度	0 ～ 7	輝度	0 ～ 8	輝度	0 ～ 7	輝度	0 ～ 8
0	00000000	0	000000000	64	01000000	88	001011000
1	00000001	1	000000001	65	01000001	89	001011001
2	00000010	2	000000010	66	01000010	91	001011011
3	00000011	3	000000011	67	01000011	92	001011100
4	00000100	4	000000100	68	01000100	93	001011101
5	00000101	5	000000101	69	01000101	95	001011111
6	00000110	6	000000110	70	01000110	96	001100000
7	00000111	8	000001000	71	01000111	98	001100010
8	00001000	9	000001001	72	01001000	99	001100011
9	00001001	11	000001011	73	01001001	100	001100100
10	00001010	12	000001100	74	01001010	102	001100110
11	00001011	13	000001101	75	01001011	103	001100111
12	00001100	15	000001111	76	01001100	104	001101000
13	00001101	16	000010000	77	01001101	106	001101010
14	00001110	17	000010001	78	01001110	107	001101011
15	00001111	19	000010011	79	01001111	109	001101101
16	00010000	20	000010100	80	01010000	110	001101110
17	00010001	22	000010110	81	01010001	111	001101111
18	00010010	23	000010111	82	01010010	113	001110001
19	00010011	24	000011000	83	01010011	114	001110010
20	00010100	26	000011010	84	01010100	115	001110011
21	00010101	27	000011011	85	01010101	117	001110101
22	00010110	28	000011100	86	01010110	118	001110110
23	00010111	30	000011110	87	01010111	120	001111000
24	00011000	31	000011111	88	01011000	121	001111001
25	00011001	33	000100001	89	01011001	122	001111010
26	00011010	34	000100010	90	01011010	124	001111100
27	00011011	35	000100011	91	01011011	125	001111101
28	00011100	36	000100100	92	01011100	126	001111110
29	00011101	36	000100100	93	01011101	128	010000000
30	00011110	37	000100101	94	01011110	129	010000001
31	00011111	38	000100110	95	01011111	131	010000011
32	00100000	40	000101000	96	01100000	132	010000100
33	00100001	41	000101001	97	01100001	133	010000101
34	00100010	42	000101010	98	01100010	135	010000111
35	00100011	44	000101100	99	01100011	136	010001000
36	00100100	45	000101101	100	01100100	138	010001010
37	00100101	46	000101110	101	01100101	139	010001011
38	00100110	48	000110000	102	01100110	140	010001100
39	00100111	49	000110001	103	01100111	142	010001110
40	00101000	50	000110010	104	01101000	143	010001111
41	00101001	51	000110011	105	01101001	144	010010000
42	00101010	52	000110100	106	01101010	146	010010010
43	00101011	53	000110101	107	01101011	147	010010011
44	00101100	55	000110111	108	01101100	149	010010101
45	00101101	56	000111000	109	01101101	150	010010110
46	00101110	57	000111001	110	01101110	151	010010111
47	00101111	59	000111011	111	01101111	153	010011001
48	00110000	60	000111100	112	01110000	154	010011010
49	00110001	62	000111110	113	01110001	155	010011011
50	00110010	63	000111111	114	01110010	157	010011101
51	00110011	64	01000000	115	01110011	158	010011110
52	00110100	66	001000010	116	01110100	160	010100000
53	00110101	67	001000011	117	01110101	161	010100001
54	00110110	69	001000101	118	01110110	162	010100010
55	00110111	70	001000110	119	01110111	164	010100100
56	00111000	71	001000111	120	01111000	165	010100101
57	00111001	73	001001001	121	01111001	167	010100111
58	00111010	74	001001010	122	01111010	168	010101000
59	00111011	75	001001011	123	01111011	169	010101001
60	00111100	77	001001101	124	01111100	171	010101011
61	00111101	78	001001110	125	01111101	172	010101100
62	00111110	80	001010000	126	01111110	173	010101101
63	00111111	81	001010001	127	01111111	175	010101111

[Drawing 24]

D_{BL}		HD_P		D_{BL}		HD_P	
輝度	0 ～ 7	輝度	0 ～ 8	輝度	0 ～ 7	輝度	0 ～ 8
128	10000000	176	010110000	192	11000000	265	100001001
129	10000001	178	010110010	193	11000001	266	100001010
130	10000010	179	010110011	194	11000010	267	100001011
131	10000011	180	010110100	195	11000011	269	100001101
132	10000100	182	010110110	196	11000100	270	100001110
133	10000101	183	010110111	197	11000101	271	100001111
134	10000110	184	010111000	198	11000110	273	100010001
135	10000111	186	010111010	199	11000111	274	100010010
136	10001000	187	010111011	200	11001000	276	100010100
137	10001001	189	010111101	201	11001001	277	100010101
138	10001010	190	010111110	202	11001010	278	100010110
139	10001011	191	010111111	203	11001011	280	100011000
140	10001100	193	011000001	204	11001100	281	100011001
141	10001101	194	011000010	205	11001101	282	100011010
142	10001110	196	011000100	206	11001110	284	100011100
143	10001111	197	011000101	207	11001111	285	100011101
144	10010000	198	011000110	208	11010000	287	100011111
145	10010001	200	011001000	209	11010001	288	100100000
146	10010010	201	011001001	210	11010010	289	100100001
147	10010011	202	011001010	211	11010011	291	100100011
148	10010100	204	011001100	212	11010100	292	100100100
149	10010101	205	011001101	213	11010101	294	100100110
150	10010110	207	011001111	214	11010110	295	100100111
151	10010111	208	011010000	215	11010111	296	100101000
152	10011000	209	011010001	216	11011000	298	100101010
153	10011001	211	011010011	217	11011001	299	100101011
154	10011010	212	011010100	218	11011010	300	100101100
155	10011011	213	011010101	219	11011011	302	100101110
156	10011100	215	011010111	220	11011100	303	100101111
157	10011101	216	011011001	221	11011101	305	100110001
158	10011110	218	011011010	222	11011110	306	100110010
159	10011111	219	011011011	223	11011111	307	100110011
160	10100000	220	011011100	224	11100000	309	100110101
161	10100001	222	011011110	225	11100001	310	100110110
162	10100010	223	011011111	226	11100010	311	100110111
163	10100011	225	011100001	227	11100011	313	100111001
164	10100100	226	011100010	228	11100100	314	100111001
165	10100101	227	011100011	229	11100101	316	100111100
166	10100110	229	011100101	230	11100110	317	100111101
167	10100111	230	011100110	231	11100111	318	100111110
168	10101000	231	011100111	232	11101000	320	101000000
169	10101001	233	011101001	233	11101001	321	101000001
170	10101010	234	011101010	234	11101010	323	101000011
171	10101011	236	001101100	235	11101011	324	101000100
172	10101100	237	011101101	236	01101100	325	101000101
173	10101101	238	011101110	237	11101101	327	101000111
174	10101110	240	011110000	238	11101110	328	101001000
175	10101111	241	011110001	239	11101111	329	101001001
176	10110000	242	011110010	240	11110000	331	101001011
177	10110001	244	011110100	241	11110001	332	101001100
178	10110010	245	011110101	242	11110010	334	101001110
179	10110011	247	011110111	243	11110011	335	101001111
180	10110100	248	011111000	244	11110100	336	101010000
181	10110101	249	011111001	245	11110101	338	101010010
182	10110110	251	011111011	246	11110110	339	101010011
183	10110111	252	011111100	247	11110111	340	101010100
184	10111000	253	011111101	248	11111000	342	101010110
185	10111001	255	011111111	249	11111001	343	101010111
186	10111010	256	100000000	250	11111010	345	101011001
187	10111011	258	100000010	251	11111011	356	101011010
188	10111100	259	100000011	252	11111100	347	101011011
189	10111101	260	100000100	253	11111101	349	101011101
190	10111110	262	100000110	254	11111110	350	101011110
191	10111111	263	100000111	255	11111111	352	101100000

[Drawing 25]

[選択消去]

Ds	HD														1フィールドにおける発光駆動パターン														発光輝度
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	SF 1	SF 2	SF 3	SF 4	SF 5	SF 6	SF 7	SF 8	SF 9	SF 10	SF 11	SF 12	SF 13	SF 14	
00000	1	0	0	0	0	0	1	0	0	0	0	0	0	0	●						●								0
00001	0	1	0	0	0	0	1	0	0	0	0	0	0	0	○	●					●								1
00010	0	0	1	0	0	0	1	0	0	0	0	0	0	0	○	○	●				●								2
00011	0	0	0	1	0	0	1	0	0	0	0	0	0	0	○	○	○	●			●								3
00100	0	0	0	0	1	0	1	0	0	0	0	0	0	0	○	○	○	○	●		●								6
00101	0	0	0	0	0	1	1	0	0	0	0	0	0	0	○	○	○	○	○	●	●								9
00110	0	0	0	0	0	0	1	0	0	0	0	0	0	0	○	○	○	○	○	○	●								17
00111	0	0	0	0	0	1	0	1	0	0	0	0	0	0	○	○	○	○	○	●	○	●							22
01000	0	0	0	0	0	0	0	1	0	0	0	0	0	0	○	○	○	○	○	○	○	●							30
01001	0	0	0	0	0	1	0	0	1	0	0	0	0	0	○	○	○	○	○	●	○	○	●						37
01010	0	0	0	0	0	0	0	0	1	0	0	0	0	0	○	○	○	○	○	○	○	○	●						45
01011	0	0	0	0	0	1	0	0	0	1	0	0	0	0	○	○	○	○	○	●	○	○	○	●					57
01100	0	0	0	0	0	0	0	0	0	1	0	0	0	0	○	○	○	○	○	○	○	○	○	●					65
01101	0	0	0	0	0	1	0	0	0	0	1	0	0	0	○	○	○	○	○	●	○	○	○	○	●				82
01110	0	0	0	0	0	0	0	0	0	0	1	0	0	0	○	○	○	○	○	○	○	○	○	○	●				90
01111	0	0	0	0	0	1	0	0	0	0	0	1	0	0	○	○	○	○	○	●	○	○	○	○	○	●			113
10000	0	0	0	0	0	0	0	0	0	0	0	1	0	0	○	○	○	○	○	○	○	○	○	○	○	●			121
10001	0	0	0	0	0	1	0	0	0	0	0	0	1	0	○	○	○	○	○	●	○	○	○	○	○	○	●		150
10010	0	0	0	0	0	0	0	0	0	0	0	0	1	0	○	○	○	○	○	○	○	○	○	○	○	○	●		158
10011	0	0	0	0	1	0	0	0	0	0	0	0	0	1	○	○	○	○	●		○	○	○	○	○	○	○	●	195
10100	0	0	0	0	0	0	0	0	0	0	0	0	0	1	○	○	○	○	○	○	○	○	○	○	○	○	○	●	206
10101	0	0	0	0	1	0	0	0	0	0	0	0	0	0	○	○	○	○	●		○	○	○	○	○	○	○	○	245
10110	0	0	0	0	0	0	0	0	0	0	0	0	0	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	256

黒丸:選択消去放電
白丸:発光

[Drawing 27]

[選択消去]

Ds	HD														1フィールドにおける発光駆動パターン														発光輝度
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	SF 1	SF 2	SF 3	SF 4	SF 5	SF 6	SF 7	SF 8	SF 9	SF 10	SF 11	SF 12	SF 13	SF 14	
0000	1	0	1	0	0	0	0	0	0	0	0	0	0	0	●		●												0
0001	0	1	0	1	0	0	0	0	0	0	0	0	0	0	○	●		●											1
0010	0	0	1	0	1	0	0	0	0	0	0	0	0	0	○	○	●		●										4
0011	0	0	0	1	0	1	0	0	0	0	0	0	0	0	○	○	○	●		●									9
0100	0	0	0	0	1	0	1	0	0	0	0	0	0	0	○	○	○	○	●		●								17
0101	0	0	0	0	0	1	0	1	0	0	0	0	0	0	○	○	○	○	○	●		●							27
0110	0	0	0	0	0	0	1	0	1	0	0	0	0	0	○	○	○	○	○	○	●		●						40
0111	0	0	0	0	0	0	0	1	0	1	0	0	0	0	○	○	○	○	○	○	○	●		●					56
1000	0	0	0	0	0	0	0	0	1	0	1	0	0	0	○	○	○	○	○	○	○	○	●		●				75
1001	0	0	0	0	0	0	0	0	0	1	0	1	0	0	○	○	○	○	○	○	○	○	○	●		●			97
1010	0	0	0	0	0	0	0	0	0	0	1	0	1	0	○	○	○	○	○	○	○	○	○	○	●		●		122
1011	0	0	0	0	0	0	0	0	0	0	0	1	0	1	○	○	○	○	○	○	○	○	○	○	○	●		●	150
1100	0	0	0	0	0	0	0	0	0	0	0	0	1	0	○	○	○	○	○	○	○	○	○	○	○	○	●		182
1101	0	0	0	0	0	0	0	0	0	0	0	0	0	1	○	○	○	○	○	○	○	○	○	○	○	○	○	●	217
1110	0	0	0	0	0	0	0	0	0	0	0	0	0	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	256

黒丸:選択消去放電
白丸:発光

[Drawing 26]

[選択消去]

Ds	HD														1フィールドにおける発光駆動パターン														発光輝度
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	SF 1	SF 2	SF 3	SF 4	SF 5	SF 6	SF 7	SF 8	SF 9	SF 10	SF 11	SF 12	SF 13	SF 14	
0000	1	1	0	0	0	0	0	0	0	0	0	0	0	0	●	●													0
0001	0	1	1	0	0	0	0	0	0	0	0	0	0	0	○	●	●												1
0010	0	0	1	1	0	0	0	0	0	0	0	0	0	0	○	○	●	●											4
0011	0	0	0	1	1	0	0	0	0	0	0	0	0	0	○	○	○	●	●										9
0100	0	0	0	0	1	1	0	0	0	0	0	0	0	0	○	○	○	○	●	●									17
0101	0	0	0	0	0	1	1	0	0	0	0	0	0	0	○	○	○	○	○	●	●								27
0110	0	0	0	0	0	0	1	1	0	0	0	0	0	0	○	○	○	○	○	○	●	●							40
0111	0	0	0	0	0	0	0	1	1	0	0	0	0	0	○	○	○	○	○	○	○	●	●						56
1000	0	0	0	0	0	0	0	0	1	1	0	0	0	0	○	○	○	○	○	○	○	○	●	●					75
1001	0	0	0	0	0	0	0	0	0	1	1	0	0	0	○	○	○	○	○	○	○	○	○	●	●				97
1010	0	0	0	0	0	0	0	0	0	0	1	1	0	0	○	○	○	○	○	○	○	○	○	○	●	●			122
1011	0	0	0	0	0	0	0	0	0	0	0	1	1	0	○	○	○	○	○	○	○	○	○	○	○	●	●		150
1100	0	0	0	0	0	0	0	0	0	0	0	0	1	1	○	○	○	○	○	○	○	○	○	○	○	○	●	●	182
1101	0	0	0	0	0	0	0	0	0	0	0	0	0	1	○	○	○	○	○	○	○	○	○	○	○	○	○	●	217
1110	0	0	0	0	0	0	0	0	0	0	0	0	0	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	256

黒丸:選択消去放電
白丸:発光

[Drawing 28]

[選択消去]

Ds	HD														1フィールドにおける発光駆動パターン														発光輝度
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	SF 1	SF 2	SF 3	SF 4	SF 5	SF 6	SF 7	SF 8	SF 9	SF 10	SF 11	SF 12	SF 13	SF 14	
0000	1	1	*	*	*	*	*	*	*	*	*	*	*	*	●	●	△	△	△	△	△	△	△	△	△	△	△	△	0
0001	0	1	1	*	*	*	*	*	*	*	*	*	*	*	○	●	●	△	△	△	△	△	△	△	△	△	△	△	1
0010	0	0	1	1	*	*	*	*	*	*	*	*	*	*	○	○	●	●	△	△	△	△	△	△	△	△	△	△	4
0011	0	0	0	1	1	*	*	*	*	*	*	*	*	*	○	○	○	●	●	△	△	△	△	△	△	△	△	△	9
0100	0	0	0	0	1	1	*	*	*	*	*	*	*	*	○	○	○	○	●	●	△	△	△	△	△	△	△	△	17
0101	0	0	0	0	0	1	1	*	*	*	*	*	*	*	○	○	○	○	○	●	●	△	△	△	△	△	△	△	27
0110	0	0	0	0	0	0	1	1	*	*	*	*	*	*	○	○	○	○	○	○	●	●	△	△	△	△	△	△	40
0111	0	0	0	0	0	0	0	1	1	*	*	*	*	*	○	○	○	○	○	○	○	●	●	△	△	△	△	△	56
1000	0	0	0	0	0	0	0	0	1	1	*	*	*	*	○	○	○	○	○	○	○	○	●	●	△	△	△	△	75
1001	0	0	0	0	0	0	0	0	0	1	1	*	*	*	○	○	○	○	○	○	○	○	○	●	●	△	△	△	97
1010	0	0	0	0	0	0	0	0	0	0	1	1	*	*	○	○	○	○	○	○	○	○	○	○	●	●	△	△	122
1011	0	0	0	0	0	0	0	0	0	0	0	1	1	*	○	○	○	○	○	○	○	○	○	○	○	●	●	△	150
1100	0	0	0	0	0	0	0	0	0	0	0	0	1	1	○	○	○	○	○	○	○	○	○	○	○	○	●	●	182
1101	0	0	0	0	0	0	0	0	0	0	0	0	0	1	○	○	○	○	○	○	○	○	○	○	○	○	○	●	217
1110	0	0	0	0	0	0	0	0	0	0	0	0	0	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	256

黒丸:選択消去放電
白丸:発光

[Drawing 29]

[選択消去]

D_S	HD														1フィールドにおける発光駆動パターン														発光輝度
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	SF 1	SF 2	SF 3	SF 4	SF 5	SF 6	SF 7	SF 8	SF 9	SF 10	SF 11	SF 12	SF 13	SF 14	
00000	1	1	0	0	0	0	1	1	0	0	0	0	0	0	●	●					●	●							0
00001	0	1	1	0	0	0	1	1	0	0	0	0	0	0	○	●	●				●	●							1
00010	0	0	1	1	0	0	1	1	0	0	0	0	0	0	○	○	●	●			●	●							2
00011	0	0	0	1	1	0	1	1	0	0	0	0	0	0	○	○	○	●	●		●	●							3
00100	0	0	0	0	1	1	1	1	0	0	0	0	0	0	○	○	○	○	●	●	●	●							6
00101	0	0	0	0	0	1	1	1	0	0	0	0	0	0	○	○	○	○	○	●	●	●							9
00110	0	0	0	0	0	0	1	1	0	0	0	0	0	0	○	○	○	○	○	○	●	●							17
00111	0	0	0	0	0	1	0	1	1	0	0	0	0	0	○	○	○	○	○	●	○	●	●						22
01000	0	0	0	0	0	0	0	1	1	0	0	0	0	0	○	○	○	○	○	○	○	●	●						30
01001	0	0	0	0	0	1	0	0	1	1	0	0	0	0	○	○	○	○	○	●	○	○	●	●					37
01010	0	0	0	0	0	0	0	0	1	1	0	0	0	0	○	○	○	○	○	○	○	○	●	●					45
01011	0	0	0	0	0	1	0	0	0	1	1	0	0	0	○	○	○	○	○	●	○	○	○	●	●				57
01100	0	0	0	0	0	0	0	0	0	1	1	0	0	0	○	○	○	○	○	○	○	○	○	●	●				65
01101	0	0	0	0	0	1	0	0	0	0	1	1	0	0	○	○	○	○	○	●	○	○	○	○	●	●			82
01110	0	0	0	0	0	0	0	0	0	0	1	1	0	0	○	○	○	○	○	○	○	○	○	○	●	●			90
01111	0	0	0	0	0	1	0	0	0	0	0	1	1	0	○	○	○	○	○	●	○	○	○	○	○	●	●		113
10000	0	0	0	0	0	0	0	0	0	0	0	1	1	0	○	○	○	○	○	○	○	○	○	○	○	●	●		121
10001	0	0	0	0	0	1	0	0	0	0	0	0	1	1	○	○	○	○	○	●	○	○	○	○	○	○	●	●	150
10010	0	0	0	0	0	0	0	0	0	0	0	0	1	1	○	○	○	○	○	○	○	○	○	○	○	○	●	●	158
10011	0	0	0	0	1	1	0	0	0	0	0	0	0	1	○	○	○	○	●	●	○	○	○	○	○	○	○	●	195
10100	0	0	0	0	0	0	0	0	0	0	0	0	0	1	○	○	○	○	○	○	○	○	○	○	○	○	○	●	206
10101	0	0	0	0	1	1	0	0	0	0	0	0	0	0	○	○	○	○	●	●	○	○	○	○	○	○	○	○	245
10110	0	0	0	0	0	0	0	0	0	0	0	0	0	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	256

黒丸:選択消去放電
白丸:発光

[Translation done.]